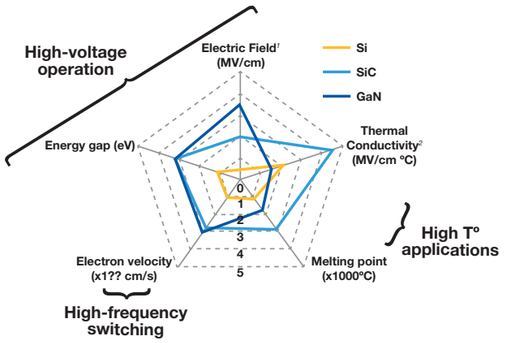
SiC – POWERING AHEAD IN POWER DEVICES

Evatec's Semicondoctor BU process engineering specialists ***Dr. Bernd Heinz*** and ***Gerald Feistritzer*** remind us why Wide Band Gap (WBG) materials like SiC have an exciting role to play in emerging power device applications. They explain how Evatec can leverage its know-how from many years experience on silicon and add new processes like carbon cap layers to help its customers power ahead in SiC technology on CLUSTERLINE®.

The benefits of Silicon Carbide

In the past decades power semiconductor technology was dominated by Si based devices, but due to its physical properties it seems that Si is reaching its performance limits and that's where wideband materials like SiC could step in. As highlighted in Figure 1, SiC offers three times the band gap of Si, about ten times the dielectric breakdown voltage and significantly better thermal properties like higher melting point and thermal conductivity.



- SiC will remain the preferred choice for high-temperature applications
- GaN could possibly reach high-voltage values, but would require bulk GaN as the substrate - which is not currently possible
- Silicon cannot compete in the high-frequency range

[1] *The electrical field profile can also be controlled by the doping concentration*

[2] *The Tc for GaN is given here for typical GaN-on-Si. It has been demonstrated that the Tc of bulk GaN could reach four W/cm °C*

Figure 1: Relative merits of Si, SiC and GaN. Ref: Yole Power GaN 2016: Epitaxy, Devices Applications and Technology Trends

Evatec – your proven industry partner

Evatec can look back with pride on its long experience in the field of Backside Metallization (BSM) coating on Si technology as a leading supplier of deposition equipment and processes for BSM on thinned wafers where the frontside processing is completed. Our knowledge has helped customers handle these substrates with excellent temperature control even where wafers have significant warpage without harming the frontside structures.

Another typical application in Si technology is trench filling with thick Al(Si,Cu) contacts. The challenges are the sidewall and bottom coverage with Ti and TiN wetting and barrier layers, followed by the subsequent void free filling of the trenches with Al in order to form a planar surface. Some typical backside and frontside processes and the know-how which Evatec offers are shown in Figures 2a, 2b and 2c respectively.

Now we can also leverage all this experience to support customers ramping up their SiC technology.

The new generation CLUSTERLINE® family delivers even more

Our new CLUSTERLINE® 200 Platform is the right choice for our customers with the capability to handle wafers up to 8 inch supporting a whole array of different power device applications. It builds on the reputation of the previous CLUSTERLINE® 200 II, and extends performance even further with various new improvements including:

- Modular architecture (Configurable with Batch Process Module, Single Process Module (PVD, PVE, PECVD, etc.))
- Upgraded component design offering increased standardization
- Increased process capability
- Enhanced tool uptime combined with reduced cost of maintenance and service
- Upgraded user interface with Evatec XPERIENCE Software
- Standardized and improved component design

We may have made lots of improvements but existing tool customers don't need to wory about compatibility. The new tool uses identical process kits as the previous CLUSTERLINE® 200 II generation (e.g. chucks, shieldings, magnet systems etc.) for high process transparency.

Protective Carbon Cap Layer processes for SiC

Doping or selective doping is one of the first process steps in SiC power device production. While thermal diffusion doping is a mature technology for other materials, the high melting point of SiC and the low diffusion constant of dopants within the material makes ion implantation the only practical technology for SiC doping. High temperature annealing at ~1600°C is a necessary process step after implantation to ensure lattice damage recovery and the electrical activation of the dopants.

The formation of a high surface roughness due to the desorption of Si atoms at temperatures > 1000°C is known as a critical issue associated with the post implantation annealing process. The most efficient state-of-the-art counter measure to prevent the unwanted roughening is the coverage of the SiC surface with a protective carbon cap layer before annealing. After annealing the remaining carbon can be removed by O_2 plasma ashing or oxidation at 700°C – 800°C.

Evatec has developed a dedicated DC sputter process on the CLUSTERLINE® 200 E platform for the cost efficient deposition of carbon layers on 6'' and 8'' SiC substrates. Typical layer results and the source configuration and are shown in Figures 3a and 3b respectively.

To find out more about Evatec process solutions for power device applications on Si, SiC or GaN contact your local Evatec sales and service office.

Learn about Evatec's new CLUSTERLINE® generation.

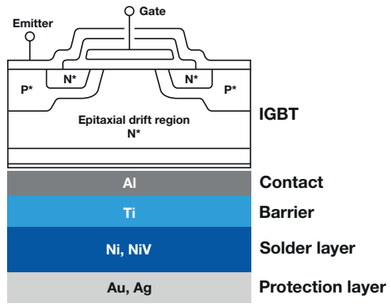


Figure 2a: Typical backside process

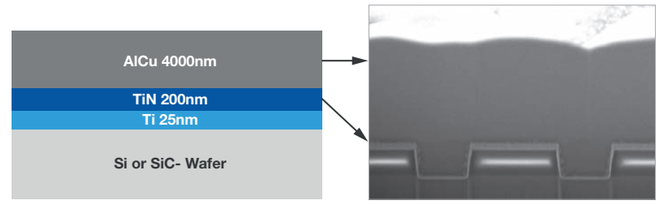


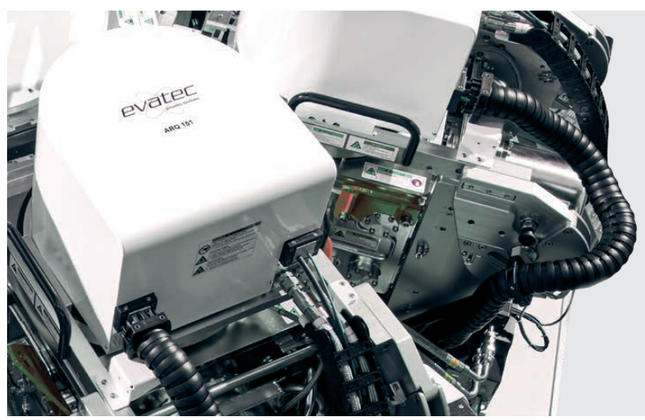
Figure 2b: Typical backside process

Process types	The Evatec Advantage
▪ PVE – Polyimide and metal removal: ICP etch	▪ Proven processes for pretreatment with Ar etch or H_2 capability
▪ PVD – Backside metallization: Al / Ti / NiV / Ni / NiSi / Au / Ag	▪ Dedicated edge grip hardware to prevent contact with finished frontside ▪ Excellent stress control capability
▪ PVD – Frontside barrier and wetting: Ti / TiN	▪ Different hardware setups available for devices based on planar or trench technology for a proper barrier layer incl. good coverage over the whole trench geometry
▪ PVD – Frontside contact: Al Flow Process	▪ High Temperature Hardware in place for trench fill and planar surface

Figure 2c: Process types and Evatec know-how

Target – Substrate Distance	50mm	125mm
Typical film thickness (nm)	20 – 400	
WiW uniformity (%)	<5%	<15%
Typical deposition rate (nm/s)	1.6	0.7
Refractice index	2.3 – 2.4	
Typical film stress (MPa)	-800 to -400	

Figure 3a: Typical layer specification for carbon capping process on 6" or 8" inch substrates



- System configuration: Single Process Modules (SPM)
- Vacuum system: Cryo-pump
- 6" or 8" chuck at room temperature
- Shadow mask (full face deposition)
- ARQ 151 DC sputtering 6kW, Ar sputter gas
- Carbon target
- Zoom shield

Figure 3b: ARQ 151 source for carbon cap deposition on CLUSTERLINE®