evatec process systems

EDITION 6

LAYERS

Extracts from LAYERS 6

Silvan Wuethrich
Head of BU Semiconductor

SEMICONDUCTOR

Strong semiconductor industry growth set to continue as Wireless filters, MEMS sensors and Power Device chips add to demand

ADVANCED PACKAGING SEMICONDUCTOR OPTOELECTRONICS PHOTONICS

SEMICONDUCTOR NEWS

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Head of BU Semiconductor

Strong semiconductor industry growth set to continue as Wireless filters, MEMS sensors and Power Device chips add to demand

Given today's rapid technological innovation, the semiconductor industry can look forward to growth. After a relatively weak 2019, we saw the semiconductor market beginning to recover in 2020 mainly in the wireless filter (5G) and MEMS sensors areas including microphone. By the end of the year the power electronics market was also seeing strong demand.

Demand for chips related to the rapidly growing use of 5G, electrical cars and also AI will contribute significantly to the industry's overall growth. The shortage of semiconductor chips is leading to major investment of the global players in 2021 and beyond into 2022.

With competition from new startups and entrants from other corners of the technology world, the race to capture the market is only intensifying. However, we are excited that our technologies and innovations are contributing to the continued growth of the semiconductor market.

I very much hope you enjoy reading the articles in this year's Semiconductor chapter.

300MM BACKSIDE METALLIZATION PROCESSES

Improved process control and productivity

The high demands on productivity and performance require the tailoring of process configurations depending on individual application needs. The versatile CLUSTERLINE® 300 PVD system for backside metallization provides dedicated configurations to optimize process results and cost of ownership. Temperature control through effective wafer cooling during deposition is a key element for this optimization. Evatec's **Gerald Feistritzer** compares the latest recessed chuck solution with electrostatic chuck (ESC) technology and demonstrates the benefits of a dedicated processing solution for thin wafers and TAIKO wafers.

The most advanced MOSFET and IGBT device architectures on ultrathin 300mm Si wafers require new levels of flexibility in equipment and process solutions for backside metallization as illustrated in figure 1.

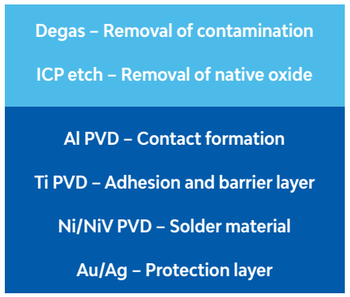


Figure 1: Typical backside metallization process sequence.

Besides the challenge of controlling the wafer bow and warpage by stress management of the layer stack, the flexibility to handle and process different substrate types is becoming more and more important. The range starts with ultrathin TAIKO Si wafers down to 60µm and continues with processing thin TAIKO wafer with tape to protect the frontside of the wafer, or alternatively the temporary bonding of Si wafers on glass with a total thickness of more than 1mm (typically with temperature limitations caused by the glue layer). Depending on the maximum allowed temperature, thermal mass of the substrate, stress, wafer bow restrictions and stress-sensitive film properties of the layer stack, CLUSTERLINE® 300 provides a solution for all these configuration options highlighting the leadership of Evatec in the power device market for backside metallization.

Managing wafer temperature and bow

Backside metallization in typical IGBT and MOSFET applications calls for deposition of thick multimetal stacks, typically Al, Ti, Ni/NiV and Au/Ag on thin 300mm wafers.

Prerequisites for processing of such high value wafers where the front side is complete with finished devices are:

- Appropriate handling of wafers without front side contact to prevent scratching / damage
- Secure highspeed handling of thin / bowed wafers
- Temperature control to prevent device damage and/or further wafer bow

Controlling the wafer temperature is not only critical, because high temperatures might create yield loss on the finished devices, but also to keep the stress of deposited films as low as possible. Stress is tuneable for most materials, for NiV for example, by pulsed sputtering and the addition of N2 gas. Keeping process temperatures low during deposition for stress control is a highly effective method for all metals, since high temperatures during deposition creates tensile thermal stress after cool-down. CLUSTERLINE® features in-situ pyrometer measurement in the PVD modules to monitor and control wafer temperature during deposition.

Increasing throughput for recessed chuck technologies

Evatec's recessed chuck solutions are well known for reliable processing of highly bowed wafers without damaging the front side. Careful process management including waiting steps is a production proven technique to avoid device damage due to overheating. However, for customers looking to improve throughput without compromizing on processing temperature CLUSTERLINE® 300 can also now be delivered with enhanced cooling options where heat exchange between wafer and chuck is increased using convection cooling.

The CLUSTERLINE® 300 with recessed chucks offers two different possible process solutions for implementing such enhanced cooling for 300mm wafers. Both are based on increasing the thermal contact with the wafer by gas convection cooling.

In so called "recessed backfill" configuration, additional argon process gas is introduced to the whole chamber in the short wait steps between sputtering to support cooling and is then pumped away prior the next sputter step (Figure 2a). An alternative configuration in figure 2b, - so called

	Process configuration			
	Recessed backfill	Recessed backgas	Recessed backgas (high T)	ESC with tape
Total process time (s)	520	381	317	310
Throughput (wph)	7.0	9.4	11.0	11.6
Wafer temperature in °C	168	169	192	90

Table 1: Throughput in wafers per hour (wph) and wafer temperature measured by Pyrometer for different process configurations. Ni deposition 1050nm, acceptable wafer bow for 120µm TAIKO: <4mm.

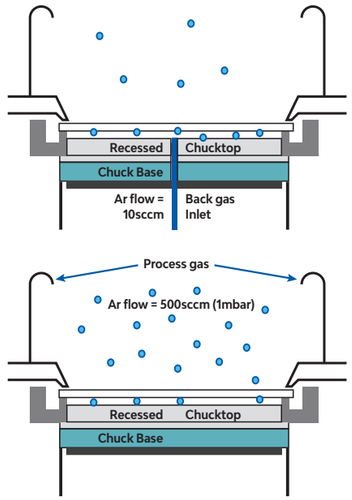


Figure 2: Comparison between recessed backfill and recessed backgas

"recessed backgas" - shows how gas is introduced via an inlet through the chuck base – the so called backgas line – to enhance the cooling step. In this configuration effective cooling can be achieved with less gas and in less time.

Figure 3 shows how the temperature quickly falls during each cooling step in a typical nickel metallization process on a 120 micron TAIKO wafer with backfill gas.

ESC vs recessed chuck technology

ESC technology with backgas offers excellent control of bow and wafer temperature while avoiding damage to the front side. An effective solution uses polyimide tape either on the wafer frontside or directly on the chuck surface. Evatec has demonstrated the excellent performance of both options on ESC based on specific customer requests.

Figure 4 shows the process temperatures measured and process times achieved for the same nickel deposition process on 300mm TAIKO wafers using ESC and different recessed chuck set ups (backfill or backgas).

We see that all solutions allow for important process performance improvements. Throughput can be enhanced using recessed chucks in either backfill or backgas configuration at a given process temperature without increasing the wafer bow. We also see how wafer throughput can be increased in production even further without impacting the bow if customers' processes allow for slightly higher peak wafer temperatures. The capability of the ESC solution to cool the wafer constantly during deposition provides the highest throughput at the lowest possible process temperatures.

Depending on the end device requirements a recessed chuck or ESC offer the best solution. Key parameters are the maximum wafer bow, substrate temperature, expected throughput and cost of ownership. With our many years of experience and servicing some of the biggest power device manufacturers in the industry we are ready to help you to find the ideal solution for your own particular needs.

The way ahead

Backside metallization is well established, but these improvements on our CLUSTERLINE® 300 can help further improve processes and their throughput. Contact us at info@evatecnet.com to find out more about our capabilities to boost performance and productivity for backside metallization.

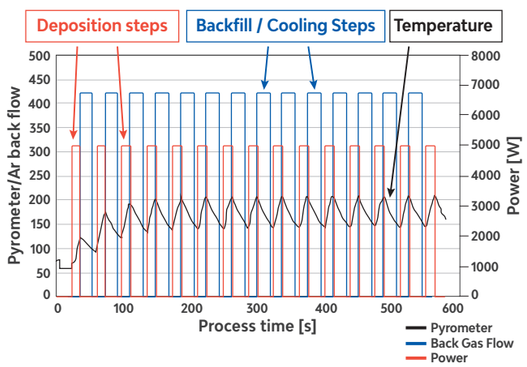


Figure 3: Temperature behaviour for a recessed backfill process.

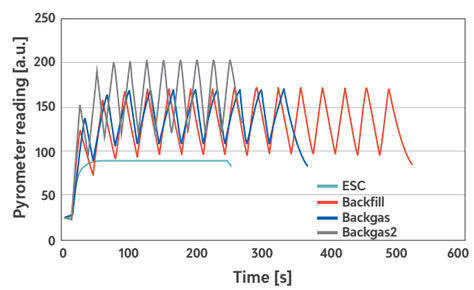


Figure 4: The comparison of different chuck configuration.

THE SKY'S THE LIMIT WITH CLUSTERLINE® 300

As we strive for increased performance and functionality of chips, back-end-of-line (BEOL) of the front-end is starting to converge with advanced packaging. Evatec's **Kai Wenz**, Senior Manager Development Projects for BU Semiconductor explains the thinking behind the release of a new front-end sputtering module on the latest variant of CLUSTERLINE® 300. Together with new platform pre-treatment features through different degassing and clean etch options, the source features include hot electrostatic clamping with active backside gas conduction heating up to 450°C, advanced power modulation and new shield design to meet particle and contamination requirements of CMOS front-end technology.

Platform

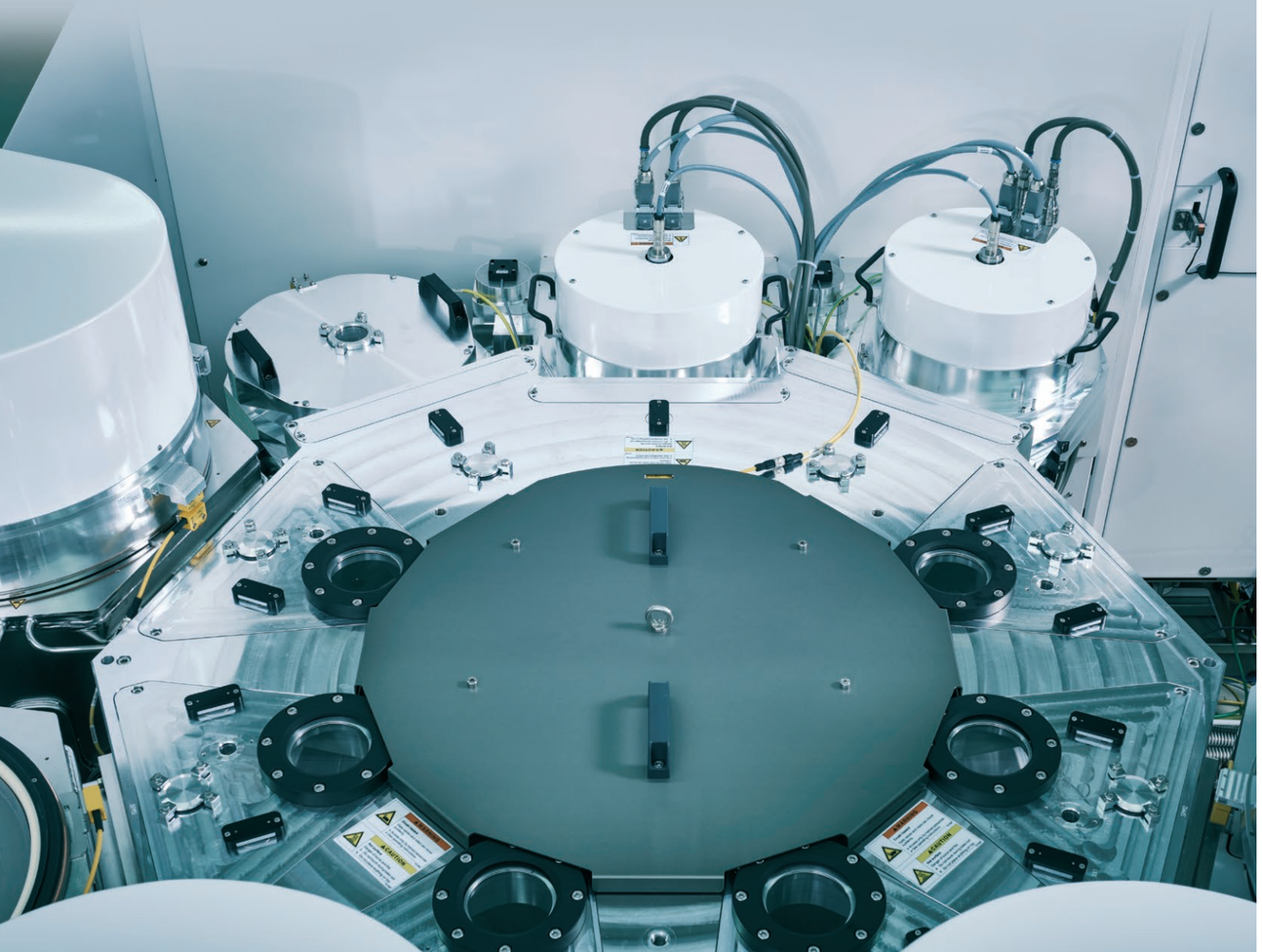
Starting with our standard high volume production CLUSTERLINE® 300 platform including existing auxiliary modules like lamp degassers and cooling plates as a baseline, we have enhanced performance by hardware design changes to achieve low metallic contamination and low particle performance. These are basic key requirements for frontside devices as structures get smaller and smaller and more sensitive. Such changes have enabled metallic contamination levels less than 1E+10 at/cm^2 and mechanical particles for size >60nm less than 15 adders (see table 1). Knowing the sensitivity of the interfaces between each process step under vacuum we have also equipped the vacuum transfer system with an additional cryogenic unit to achieve a lower base pressure <6.0E^{-8} mbar and increase the purity of the vacuum.

The atmospheric front-end of the CLUSTERLINE® 300 is equipped with a FOUP loading system capable for up to 3 FOUPs, aligner stations, buffer / dummy wafer and flipper stations based on customer needs. The aligner station is an Evatec customized unit that allows multiple wafer orientation including glass substrates.

For process pre-treatment prior to deposition we can offer our customers lamp degassers to rapidly heat up and outgas wafers up to 350°C wafer temperature and prepare it for the next process step. After processing we have the option to cool down substrates from process to room temperature before returning to the FOUP.

PVE soft-etch single wafer process module

Beside the adaptations to comply with contamination requirements we have enhanced the process shield set for tight "within wafer" uniformity performance <2.5% (max,min) for wafer cleaning and removal of oxides on the substrates. This ICP etch module has the capabilities to etch metal layers and is generally not sensitive for over etching of substrates since its equipped with a metal cage which also improves the kit life. As an option, the ICP soft-etch chamber can also be used for Ar/H2 etch process based on customer requirements in addition to conventional pure Ar etch.



Item	Ti-PVD	TiN-PVD	AlCu-PVD
Typical thickness range	100 – 120nm	100 – 200nm	100 – 5000nm
Deposition rate	3.23nm/s	1.49nm/s	9.8 - 22.6nm/s
WiW thickness uniformity (max, min)	1.30%	2.50%	2.10%
WiW RS uniformity (max, min)	1.90%	3.90%	1.90%
WtW thickness / RS uniformity (max, min)	0.30%	0.60%	0.50%
Specific resistivity	58 µΩ*cm	137 µΩ*cm	2.9 µΩ*cm
Mech. particles >0.06um >0.12um >0.96um	4 adders 0 adders 0 adders	7 adders 1 adders 0 adders	3 adders 9 adders 0 adders
In-film particles >0.2um*	14 adders	21 adders	23 adders
** without TWAS coated shields*			

PVD single wafer process module

Process modules have also been enhanced with new process shield kits with the focus on variable large range target-substrate distance capabilities, low particles and contamination, uniform gas distribution and low particle performance.

From the source side we can now offer the next generation of PVD sputter source ARQ 320 which is capable / prepared for DC, DC pulsed, RF and HIPIMS sputtering. This new sputter source allows circumference non-uniformity by advanced power modulation and radial compensation by magnet lift design.

The flexible module setup can be equipped with active Electrostatic Chuck (ESC) hot (450°C) and cold, or alternatively with clampless, passive chuck depending on the configuration and process requirements including RF chuck bias.

With these hardware features we can achieve within wafer uniformity performance <3.0% (max,min) depending on the sputter materials for physical film thickness and sheet resistance.

Customized process modules

The markets addressed by Evatec today span from discrete power devices and mixed signal power IC applications up to CMOS interconnect technology, but platform performance and flexibility open up even further opportunities with other modular options. For example, the "Multi-source" option in a single chamber allows installation of up to 4 small size targets for reduced time to market development of new materials, or co-sputtering of different materials including rotating chuck. Integration of a batch sputtering module which we typically use for optical or magnetic laminate coatings, or advanced directional sputtering with high ionized sputtering technology in combination with increased target substrate distances and biased chuck also bring even more capabilities and flexibility for the overall platform.

The sky's the limit

The new front-end module is positioned at the high end on the performance level but from a flexibility perspective the module and platform concept will meet all types of upcoming front-end integration applications. Our customers will be able to bridge the gap enjoying CMOS compatible sputtering equipment and the flexibility for heterogenous integration of RF-devices, optical or magnetic sensors or any 3D-IC application.

"With all these features Evatec enables new possibilities for our customers. We might be starting off with power applications, but we really aren't facing any limits in the future!"

POWERING AHEAD TOGETHER –

Driving up energy efficiency in Bipolar Devices

Michelle Bourke from Lam Research and **Dr. Reinhard Benz** from Evatec explain how the two companies are working together to reduce ohmic losses for higher energy efficiency in bipolar device technology by optimizing the interface to the backside metallization of thin silicon wafers. The ultimate goal is to improve the on-resistance performance of bipolar transistors for the power industry.

In today's society we often take for granted the devices behind the improved functionality we experience from electronic devices. From the consumer electronics we use day-to-day, to the realization of 5G networks and fully electric vehicles, the technology enabling them is truly fascinating.

Pausing for a second to consider this group of enabling technologies we start to see a group of devices emerge that today are known as specialty devices. These devices include MEMS and sensors, RF devices, optical components, analog and mixed signal devices, power devices and power management ICs.

While many bring experiences we can "see", such as the MEMS and sensor devices or CMOS image sensors, power devices and power management ICs are enabling improved voltage performance and speed of operation, which ultimately means better battery lifetime and faster charging.

As the ecosystem and functionality evolves, so too does the power electronics sector: from traditional, well-known applications in the photovoltaic (PV), wind, motor drivers, UPS or rail systems to new applications in electric and hybrid electric vehicles, charging stations and energy storage systems. Not only are we seeing an evolution in the traditional silicon-based devices but also the adoption of new materials such as silicon carbide (SiC) or gallium nitride (GaN).

Historically, power devices were primarily based on silicon technologies. Planar metal oxide semiconductor field effect transistors (MOSFETs) and oxide filled trench (OFT) devices typically operated in the 10s of volts to a few 100s of volts, with super junction MOSFETS (SJ MOSFETs) occupying the 500-1000V range and finally, insulated gate bipolar transistors (IGBT's) operating in the higher voltage range between a few 100s to several thousand volts. While the introduction of wideband semiconductors offers higher power coupled with higher frequency capabilities, the silicon industry continues to push the boundaries of what is possible.

The transition from traditional MOSFET devices to SJ MOSFETs allows for higher voltages with lower RDS(ON), enabling faster switching frequency. Similarly, advances in IGBT technology are addressing higher power applications. IGBT power density is increased by more densely packed trench gates separated by small, in some case sub-micron mesas and IGBT ON resistance (RON) is reduced by using increasingly thin device wafers.

As IGBT wafers become thinner and the RON from the body of the device continues to decrease, the contact resistance will play an increasingly significant role in overall device performance. As a result, engineering of the backside contact will become more important.

The capability to "engineer" the roughness of the backside pre-PVD to improve the ohmic nature of the contact and reduce the contact resistance will therefore be of great interest. At the same time, you need to avoid reducing the breakdown voltage (Vbd) due to variations in the roughness as this surface roughness becomes more significant with respect to the overall device thickness.

To address these technical challenges Evatec and Lam Research realized that working together would be a great way to accelerate innovation. As leading technology and equipment providers, we are bringing together our long-term expertise in bipolar device technology to work on surface modification and adhesion at the interface to the backside metallization of thin silicon wafers. The ultimate goal is to improve the on-resistance performance of bipolar transistors for the power industry.

Of course, there are many challenges to be addressed in optimizing the handling and processing of wafer thicknesses down to 50µm, especially in high volume manufacturing environments. Lam's Reliant® systems already have a strong track record in single wafer clean and wet etch technologies, particularly stress relief of thinned wafers to improve wafer strength as well as controlling surface roughness. Evatec has proven expertise in thin wafer handling, stress control of the solder material stack and the thermal wafer budget to control the wafer bow. We are excited by the prospect of working together to achieve important advances for bipolar technology.

Dr. David Haynes from Lam Research noted, "We are extremely pleased to be working with Evatec. This collaboration should help our customers solve some of the most pressing challenges in the advancement of power devices. Evatec's capabilities are highly complementary to those offered by Lam. By working together, we are focused on delivering integrated technical solutions that our customers are able to implement quickly with minimum development and maximum benefit. We also hope that we will be able to bring these advantages of cooperative development to bear on other applications not just in power electronics, but also other device technologies."

Evatec's Dr. Reinhard Benz noted, "Combining know-how is always a great way to accelerate innovation, and Lam Research and Evatec have started to cooperate on their long-term expertise in bipolar device technology. Together we cover all the critical process steps on ultra-thin silicon wafers and our technical solutions provide the highest security and

reliability in thin wafer processing to our customers. We are excited by what's to come and have already identified other areas where such a complementary collaboration could be very fruitful."

While it is early days in this technical collaboration, initial results have shown to be very promising. The goal is that through 2021 we will continue to share results so that the industry can have confidence in addressing the challenges they face. Stay tuned for more information!

SilTerra

Delivering high performance MEMS solutions to achieve faster time to market

Dr. Mohanraj Soundara Pandian, Deputy Director of the MEMS & SENSORS Business Unit, tells us about the MEMS activities at SilTerra and how deposition of high performance piezoelectrics like AlScN is key to SilTerra's MEMS & sensors technology roadmap.

Tell us about SilTerra and its history?

SilTerra is a pure-play 200mm global semiconductor foundry. It was set up in 1995 as a project of strategic national interest. Headquartered in the northern region of Malaysia in the state of Kedah, SilTerra also has offices in Kuala Lumpur, Taiwan and the United States.

We offer a full range of CMOS process technologies covering advanced logic, RFCMOS, mixed signal and high voltage. With these core CMOS technologies, we then progressed into More than Moore (MtM) technology areas to include silicon photonics, MEMS, IoT, advanced power and gallium nitride into our technology portfolio enabling new products for applications in life sciences, consumer electronics, mobility and data communications.

How do the company's activities fit in the Semiconductor value chain?

We produce semiconductor wafers for our customers who are essentially product companies as well as fabless design houses that serve end markets such as consumer electronics, life sciences, IoT, mobility and data communications.

Tell us about your journey into MEMS. How has it evolved?

Our journey into MEMS began in 2010. It started with the development of a customer proprietary device which was a MEMS micro-mirror chip for data projectors. With the device integrated onto our 0.18micron CMOS process platform, we were able to develop a process that was manufacturable with good yield performance.

In 2011, we progressed into developing our own MEMS-on-CMOS device architecture for RF MEMS resonators that cover a frequency range from 10MHz to 2.4GHz.

Our ultrasonic MEMS platform started in 2015, and since then we have grown in leaps and bounds in terms of expertise, capability and resources. With a design platform supported by CMOS IP and a physical design kit, our customers are able to build ultrasonic MEMS sensors on top of our CMOS/BCD/RF process platforms ranging from 180nm to 110nm. Through the years, we have fine tuned this platform, and introduced enhancements into our device fabrication process to provide more value for our customers.

Fast forward to today, we are working with over 8 global customers for applications in imaging, fingerprint sensing, in mobile as well as industrial applications. Most of these projects are at various stages of prototype development and field trials.

What is unique about the MEMS solutions developed by SilTerra?

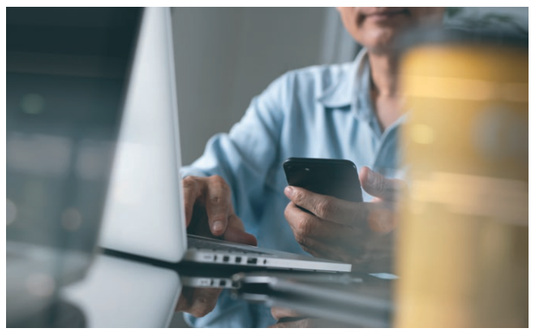
Emerging sensor applications in consumer devices, automotive, healthcare and medical markets are continuing to demand for devices that are highly versatile, miniaturized, reliable, and cost-effective. While MEMS devices are capable of addressing these demands, the cycle time for development and the cost of ownership involved for such tremendous development activities is high.

Adopting MEMS prototyping with CMOS is an effective approach. Although MEMS devices are formed using common CMOS materials such as silicon and poly-silicon, the paths to achieve microfabrication and integration are numerous, and most often require specialized tools, processes, and skilled resources.

At SilTerra, our focus is on MEMS devices using standardized manufacturing methods so that we are able to support our customers in their "go to market" strategy in a short period of time.

Please explain more about SilTerra's MEMS-on-CMOS technology platform.

As the name implies, the MEMS devices are directly fabricated on top of the CMOS layers. This form of integration is known as a monolithic integration. It is a seamless manufacturing technique in which MEMS process modules use CMOS-compatible materials and processing methodologies. Using this approach, it is easier to achieve smaller form factors of devices with reduced electrical parasitics because of the direct connection between the CMOS and MEMS structures. The fact that these devices are single-chip solutions built on well-established and mature CMOS manufacturing methods also make this technology rather cost-effective.



In consumer devices such as smartphones, MEMS technologies are expected to enable various functions ranging from gesture control, navigation and smart interfacing.

Comprehensive in-house failure analysis at SilTerra.

What are some of the devices built on this platform?

We developed a few monolithic MEMS process technologies based on the actuation methods.

The first platform is based on electrostatic actuation, where the devices have an electrostatic air gap of 90nm and are fully sealed with the thin film capping process. This approach not only lowers the actuation voltage of the device, but also makes it compatible with post packaging processes such as conventional back-grinding, dicing and high pressure molding.

The second platform is based on piezoelectric actuation. This platform has customizable process options for acoustic modes. Customers can choose to electrically enable longitudinal acoustic modes or lateral acoustic modes or a combination of both.

It is important to note that the MEMS-on-CMOS platform is well suited towards more complex applications such as micromirror arrays for projectors, bolometers for infrared imaging and ultrasonic transducers for medical imaging. These applications involve high density arrays and moving elements under the control of the CMOS readout circuits.

On the other hand, applications that may involve only a single MEMS cell or multiple MEMS cells include microphones, accelerometers and gyroscopes. As these MEMS devices are relatively simple in terms of structure, passive MEMS device manufacturing methods are adequate.

At SilTerra, we are able to address MEMS manufacturing to address both simple as well as complex requirements.

Tell us about your work in the area of thin film piezoelectrics.

PiezoMEMS is one of the core technologies in SilTerra's MEMS & Sensors technology roadmap.

The piezoelectric thin films that are in use include aluminium nitride (AlN) and scandium doped aluminium nitride (ScAlN). Some of the devices we are working on include piezoelectric micromachined ultrasonic transducers (PMUTs), surface acoustic wave (SAW) resonators, bulk acoustic wave (BAW) resonators, thin piezoelectric on silicon (TPoS) and piezoelectric actuated micromirrors (PAM).

What are some of the thin film manufacturing challenges that you have had to solve?

The challenge we see is mainly in the process integration of piezoelectric thin films.

To begin with, the deposition of high quality piezoelectric thin films is of extreme importance to us in the fabrication of piezoMEMS devices. We need to ensure that the growth of films is controlled within tight specifications for uniformity and repeatability. This is where the strength of Evatec lies, ie. in providing us with high quality thin film deposition technology that meets these requirements.

As part of MEMS device development, we need to investigate the interaction between the thin films and other stacks and process modules in terms of stress. The very nature of MEMS technology usually demands balancing many material or film properties. Finding the right manufacturing method that ensures the best stress uniformities while maintaining good thickness uniformity is key to achieving both best signal-to-noise ratio and coupling coefficients.

How do you work together with equipment suppliers like Evatec?

MEMS specialty tools, materials and process recipes are always evolving. The needs of the industry are also very dynamic, hence we are always on the lookout to understand the market needs and the potential technologies that are available to address these needs.

Our partnership with Evatec began in 2017. The growth we have experienced from this partnership has been mutual. In the early stages of the partnership, we worked closely with Evatec on an engineering job basis to develop and customize piezoelectric thin films to suit our process integration methods, as it was impractical to invest in tools during device conceptualization itself. Evatec was very supportive of us right from the beginning. With the growth of our technology platform, the decision to utilize Evatec's tool was an easy one, given the strong customer support that we received from Evatec, combined with excellent tool performance that met our thin film deposition needs.

How is Evatec's technology helping you today?

Today we use Evatec's CLUSTERLINE® 200 II mainly for the deposition of aluminum nitride and aluminum scandium nitride. We also use it for ion etch, which is a pre-etch step to prepare the surface for deposition.

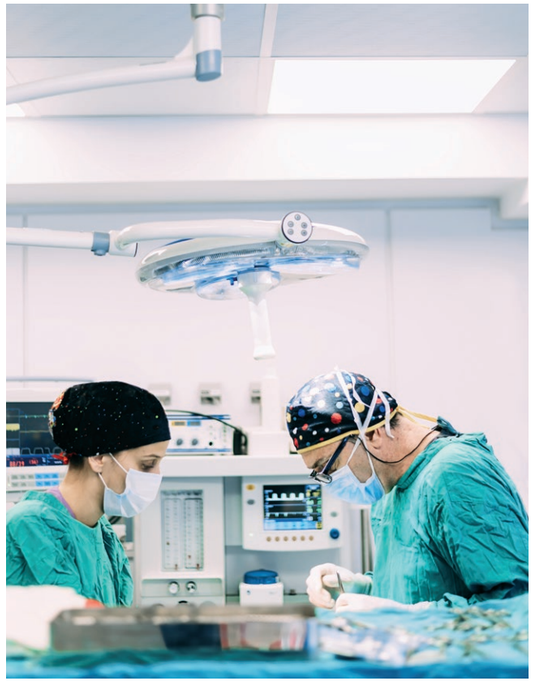
One might think depositing the bulk piezo layer is the most critical part of such a device. In fact, the truth is "buried underneath", as optimal nucleation is the key for the desired crystallinity of these materials. Providing the right template or seed is an integral part of the expertise to master this challenge and the pre-etch step is one of the ingredients for that.

What new things do you hope the tool will help you do in the future?

Currently we are using up to 9.5% of scandium concentration in aluminium nitride. We expect this percentage to go up to 20% and beyond in the near future for the development of our MEMS devices.

How do you see the market for piezoelectric MEMS devices developing?

We are seeing significant impetus from customers in various domains such as consumer electronics, industrial applications and healthcare.



In healthcare, MEMS technologies enable medical imaging and diagnostics applications.

User interface technologies in consumer electronics devices are rapidly evolving with touch screen, gesture control and superior authentication features. There is also strong interest to implement gesture control in cars so that drivers are able to control or select specific features without needing to manually press any buttons. All these interfaces will strongly leverage on MEMS based ultrasonic sensors which act as haptic sensors, proximity sensors and fingerprint sensors.

PiezoMEMS devices will also be raising the bar for 3D ultrasonic imaging and field inspection applications over the next few years.

The other area which is witnessing strong interest in MEMS devices is in resonator technologies for timing and radio-frequency applications.

What are some of the expectations from your customers with regard to MEMS devices?

Our customers expect us to offer them a technology platform which is robust in terms of device performance, yield, reliability and manufacturability. Cost effectiveness is also an important factor. The fact that our MEMS integrated solutions are single-chip and monolithic is already an advantage for our customers in terms of cost effectiveness. Our customers are also looking to ramp up their product into volume manufacturing in a short timeframe.

Ultrasonic Devices			Acoustic Devices	
100KHz - 200KHz	400KHz - 1MHz	3MHz - 40MHz	200MHz - 1GHz	2GHz - 3GHz
Proximity sensors	Haptic sensors	Medical imaging fingerprint	Timing	RF Sensing

Demonstrated devices on SilTerra's PiezoMEMS platform.

What do you foresee happening in the MEMS scene in the short term future and how is SilTerra geared towards it?

Increased customization in MEMS devices is something that we expect to see. Each application and device is unique, so we need to ensure we maintain specific thickness of piezo layers while balancing a whole lot of other factors to trim different figures of merit to the maximum. While ultrasonic transducers, speakers or microphones are finally measured by their signal-to-noise ratio, RF-MEMS such as BAW filters are built around optimized coupling. Energy scavengers are different again and all of them need to be compared against their respective quality factors in the end. What we need is therefore not only the theory at hand, but also a tool that allows us to operate the knobs and control these properties. Evatec's CLUSTERLINE® 200 provides us the flexibility to balance these factors while maintaining the device at optimum performance levels.

> **With the growth of our technology platform, the decision to utilize Evatec's tool was an easy one, given the strong customer support that we received from Evatec**

To a certain extent, we foresee and plan our engineering demonstrations to closely meet the needs of our customers. For ultrasonics, we have demonstrated a number of devices such as proximity sensors (100 to 200kHz), haptic sensors (400kHz to 1MHz) and sensors for medical imaging and fingerprint (3 to 40MHz). For acoustic devices, we have demonstrated devices for timing applications (200MHz to 1GHz) and for RF sensing applications (2GHz to 3GHz).

Through our partnership with Evatec, we are looking into enhancing piezoelectric responses for our MEMS devices using higher concentrations of scandium. We are also looking into the integration of ferroelectric thin films on MEMS devices. These efforts are currently at proof of concept stage.

With the right set of process tools and capabilities, we are in a good position to deliver the best solutions to our customers while helping them achieve quick time to market.

About the author

Dr. Mohanraj is responsible for the development of the MEMS product portfolio at SilTerra. He leads the team in integrating MEMS devices with CMOS which includes developing capabilities to bring a MEMS device from conceptual stage right up to volume manufacturing. Prior to SilTerra, Dr. Mohanraj held senior engineering roles in developing silicon based process technologies in the MEMS, TSV and advanced packaging fields. He holds a PhD in Mechanical Engineering from the National University of Singapore. He has authored and co-authored more than 30 research publications and holds 4 US patents in MEMS development.

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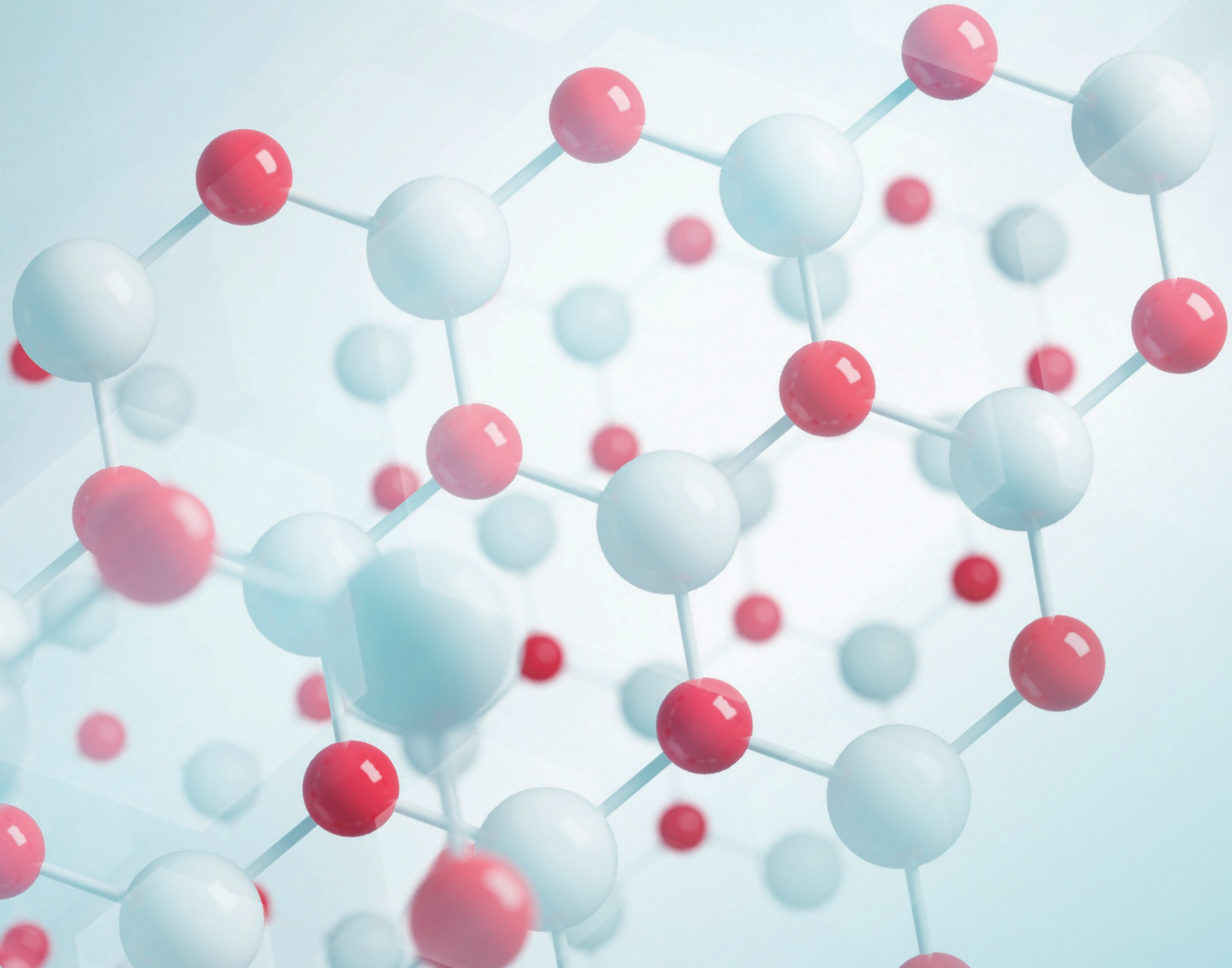
AlScN THIN FILM TECHNOLOGY
Where are we today?

There has been huge progress over the last few years in developing high performance piezoelectric materials like aluminum scandium nitride. Evatec's **Dr. Andrea Mazzalai** takes a moment to remind us of what they offer in comparison with other materials and the technical challenges in their deposition with specific focus on the manufacturing of bulk acoustic wave (BAW) resonator based filters for radio communication. The advances in physical vapor deposition (PVD) techniques are also summarized and results reported showing that defect densities and stress can be kept well within the required ranges for successful device production.



Introduction

The widespread application of small, cheap and energy efficient devices introducing new functionalities into wearable systems has changed our lifestyle during the last decades. At the heart of this revolution, we find the so called "MEMS", an acronym standing for micro electromechanical systems. Motion control or detection of sub millimeter size mechanical parts is possible with inexpensive electronics exploiting several physical material properties.

Among them, piezoelectricity based devices (piezo-MEMS) have been successfully employed to produce actuators (miniaturized pumps or loudspeakers), transducers (for ultrasound imaging), sensors (microphones and ultrasound detectors) and resonators.

Whenever low signal-to-noise ratios or low losses are needed, aluminum nitride (AlN) is the material of choice.

Characterized by a Wurtzite structure, AlN is also characterized by excellent stability of its spontaneous polarization and by very low dielectric losses compared with other compounds. The disadvantage, however, is that the piezoelectric activity is small in comparison with ferroelectrics. Materials scientists have devoted considerable efforts to improve the properties of AlN films by exploring the effects of statistical substitution of Al with other elements of the periodic table. It is in this context that Akyiama and co-workers [1] reported a dramatic increase in the piezoelectric coefficient when scandium atoms replaced aluminum ones up to approximately 43% in 2009. As we can see from the dashed line in figure 1, the experimental data can be reasonably fitted with a linear trend.

These experimental results had their foundation in ab-initio calculations of crystal lattice properties. As reported by Tasnadi et al. [2] the lattice parameter c/a gets progressively smaller with Sc substitution and with it comes a reduction in stiffness of the material. At the heart of this transformation, as for other piezoelectric materials, there is a structural instability: the competing tendency of pure AlN having a polar structure and of ScN showing a rocksalt, non piezoelectric arrangement of atoms. Close to the phase transition (occurring at about 43% Sc), changes in the polarization are much easier to obtain, meaning that smaller mechanical deformations are sufficient to obtain the appearance of a given amount of surface charges, which means in turn higher piezoelectric coefficient.

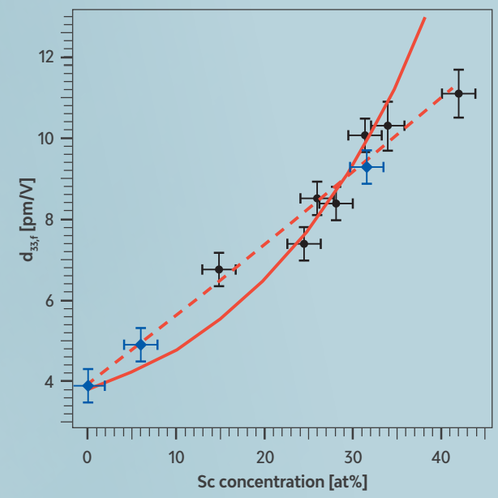


Figure 1: Effective longitudinal piezoelectric coefficient $d_{33,f}$ as a function of the Sc content. Solid red curve represents the value obtained from ab-initio calculation [3]. Black and blue points are data measured with a DBLI technique [4] out of films deposited with 4" and 12" diameter targets respectively.

This structural instability also has the effect of increasing the energy dissipation in resonators, reminding us again that there is a trade off by nature between electromechanical coupling coefficients and quality factor. However, our ability to engineer material properties is clear and we see that by selecting the appropriate Sc content we can tailor material performance to specific applications.

Technical Challenges

The very first results for deposition of $Al_{1-x}Sc_xN$ thin films were obtained from co-sputtering setups. The compositions were adjusted by calibrating the power ratio between two independent targets, one of Al and the other of Sc. Although flexible and ideal for process development, this manufacturing solution is, however, not ideal for mass production as it is very challenging to ensure adequate stress control (more about this topic later) and to achieve high levels of productivity.

The preferred solution is therefore to use the same proven configuration currently already employed for high volume fabrication of RF filters using a single target, much wider than the substrate diameter.

To do this we must employ an $Al_{1-x}Sc_xN$ alloy. Casting of ingots from melted metals is however particularly difficult, as the final product becomes brittle. As a raw material, scandium is also not available in high purity, and reducing the concentration of oxygen and other contaminants down to the levels possible in equivalent pure Al targets is an additional challenge.

As a matter of principle, however, the fabrication of such a target is feasible. The business case represented by opportunities in 5G communication has stimulated target manufacturers to make significant investments resulting in remarkable improvements throughout a whole range of Al-Sc compositions in recent years. It is now possible to produce high quality, high Sc content targets (up to 40% Sc) which enables the mass production of $Al_{1-x}Sc_xN$ throughout the whole piezoelectric range of the phase diagram.

The huge interest in Wurtzite aluminium scandium nitride thin films for RF resonators has been driven by the need for enlarging the bandwith of filters in the GHz range. We can indeed fabricate resonators with such operating frequencies out of films a few hundreds of nanometers thick. The enhanced electromechanical coupling coefficient with respect to pure aluminium nitride enlarges the frequency gap between resonance and anti-resonance peaks in the impedance spectrum.

The accurate tuning of such frequencies of several filters connected in a network can result in a band-pass filter transformation function. The larger the electromechanical coupling coefficient of each resonator, the wider the width of the band. A good filter, however, is also characterized by a very steep decrease of the impedance outside of the selected band. This high rejection of adjacent bands depends on the quality factor of each resonator and on their number in the network. In order to reduce costs, the number of resonators has to be kept to a minimum, so the technological quest is to increase the Q-factor for a given electromechanical coupling coefficient k_t^2. This is the reason why their product is the figure of merit for this application.

The Sc content is not however the only parameter which influences k_t^2, as the piezoelectric response is also influenced significantly by the film stress (see figure 2). Extremely accurate stress control within the wafer surface and from wafer to wafer in any production process is essential then for successful production of RF filters of bandwidth precision dictated by the wireless communication standards. For Sc contents of about 30% only deviations of ± 50MPa are tolerated: an extremely small value for thin film depositions.

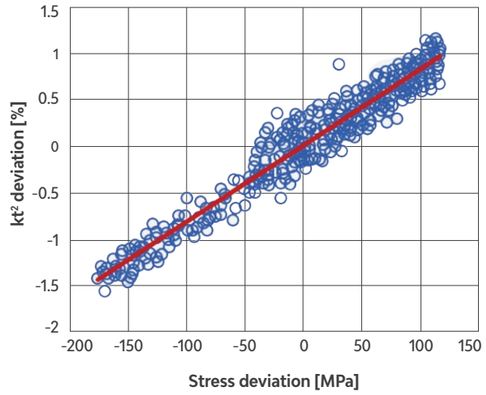


Figure 2: Electromechanical coupling coefficient variation as a function of the stress variation for $Al_{0.7}Sc_{0.3}N$ based resonators. The two physical quantities are linked linearly. The steepness of the line increases with the Sc concentration.

Recent advances in $Al_{1-x}Sc_xN$ thin film processing

In magnetron sputtering processes, a narrow range of stress distribution is achieved under conditions of homogeneous ion bombardment over the whole wafer surface. This is normally achieved at large angle conditions where the impact of the inhomogenous magnetic field of the magnetron is damped, and where the pressure distribution in the processing chamber is more uniform. However, these conditions are often associated with a large thickness inhomogeneity, which translates into large frequency dispersion of the resonators over the wafer surface. Within certain boundaries, the frequency shift can be compensated: resonators are normally fabricated with an excess of mass, and in a second step the right amout of material is removed from each resonator with accurate trimming in order to finely tune the frequency. Coupling coefficient cannot be modified, as there is no viable option to modify the stress and / or the Sc content locally. A simple approach to achieve better compromises between stress and thickness uniformities is to employ a larger target diameter (Figure 3). This allows us to reduce the strength of the magnetic field at the edges and / or to enhance the target to substrate distance for a given thickness distribution. Under both circumstances the inhomogeneity of the ion bombardment over the wafer surface is reduced, thus favoring a more uniform stress distribution.

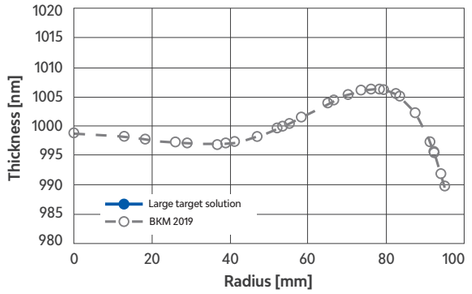


Figure 3: Comparison of deposition uniformities for different target diameters.

On the downside however, this approach worsens the cost of ownership figure as it implies a bigger vacuum chamber, larger cleanroom footprints, and, most importantly, a much higher target cost per wafer (if it is at all possible to get manufactures able to go beyond the usual target sizes for $Al_{1-x}Sc_xN$ alloys). A smarter way to deal with the issue is to manipulate the stress distribution while keeping the optimized magnetron configuration and target to substrate distance for ideal thickness distribution. This is possible with DC+RF technology.

The combination of DC+RF is also commonly used in a variety of applications for other advantages which are offered by this technique. The transfer of this mature technology to $Al_{1-x}Sc_xN$ depositions allowed us to achieve very narrow stress distributions up to the wafer edge (Figure 4), and satisfy the ± 50MPa limits requirement dictated by large amount of scandium substitution while keeping the thickness distribution easily trimmable (< 0.5% sigma/mean) and target dimensions to the conventional ones (about 300mm diameter).

The second main obstacle which arises from $Al_{1-x}Sc_xN$ thin film deposition is the tendency of these materials to show abnormally thick, misoriented crystallites or grains. These grains are still in the Wurtzite phase, but their (0002) axis is not perpendicular to the wafer surface. This causes an obvious decrease of the piezoelectric coefficient, which becomes evident only when their density exceeds a critical threshold. An excessive amount of these grains can also negatively influence the dielectric losses and can cause problems in post-processing due to the very high resulting film roughness. (Note: these grains can be tens of nanometer taller than the film surface).

As demonstrated by Sandu et al. [5], the presence of these abnormal grains can be associated with an excess of Sc at the grain boundaries. Target manufacturing and processing conditions can therefore significantly influence the presence of these grains. Sc segregation on the target surface has to be avoided, as must general conditions where the scattering of the sputtered species in the plasma is enhanced (large target-to-substrate distance or large pressures). This is also the reason why this phenomenon gets progressively more important with the increase of the Sc content. Moreover from the dynamics of Wurtzite growth we know [6] that at large angle scattering conditions the tendency of the Wurtzite films to grow perpendicularly to the film surface is reduced. However the main driver for this phenomenon is still the target manufacturing quality: ingots showing smoother surface after sputtering and superior mechanical quality tend to show less abnormally grown misoriented grains. It is worth noting that other requirements in terms of thickness and stress distribution give us very limited freedom in the choice of the scattering conditions, especially the requirement of having neutral or slightly tensile films. If we produce too compressive films the benefit of high Sc content in the Wurtzite structure is lost by the loss of coupling coefficient given by the stress state (see again figure 4). For practical reasons, it could be that the highest piezoelectric response occurrs at a lower Sc concentration than that reported by Akyiama and coworkers.

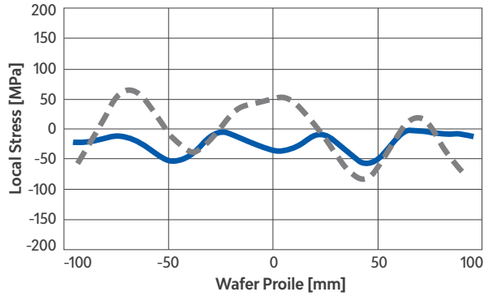


Figure 4: Comparison between stress profile with DC-pulsed process (dashed line) and DC+RF (solid line). Thanks to the additional process parameter which influences mainly the plasma distribution over the wafer surface, we achieve high levels of stress uniformity.

> From large target diameters to DC+RF technology we have flexible solutions to adjust the plasma distribution over the wafer surface

For a given target and set of processing conditions, the number of misoriented grains can also change drastically from substrate to substrate type. On bare silicon wafers it is relatively easy to grow smooth films, while the number of misoriented grains is increased if we switch to Mo or W electrodes. The lattice mismatch between the film and the substrate does not seem to be the root cause however, as the processing conditions of the electrodes have a big influence, as we can see in figure 5.

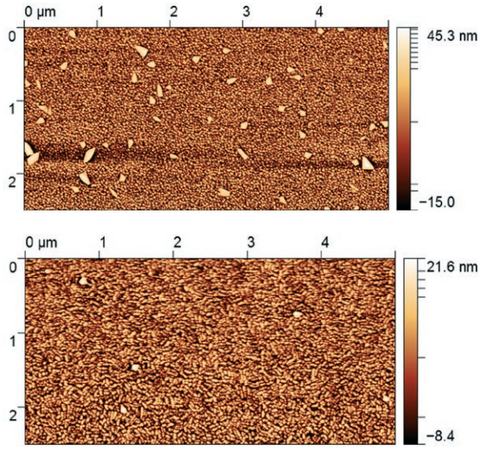


Figure 5: AFM pictograms of $Al_{0.7}Sc_{0.3}N$ thin films obtained under identical conditions on two different types of bottom electrodes. A significant reduction of the unwanted grain density can be achieved with a pre-treatment of the electrode before the piezoelectric thin film deposition.

Integration of piezoelectric thin films is limited by chemical compatibility and wafer temperature restrictions. Luckily Sc is CMOS compatible, so resonator structures can be deposited directly onto conditioning electronics in monolithic designs, reducing the form factor of devices. Thermal instability of underlying materials limit the maximum wafer temperatures to about 400°C to 450°C, also for conventional MEMS structures outside CMOS fabs. This temperature limit also forces the use of Wurtzite nitrides relative to ferroelectrics which normally have nucleation energies which require higher temperatures.

Conclusions

The integration of $Al_{1-x}S_{cx}N$ films poses several challenges. The historic difficulties in target manufacturing represented a significant hurdle in the commercialization of such technology for a long time limiting users to cosputtering setups for relatively high Sc concentrations. However, targets of 12 inches in diameter are now available for almost all the Sc concentration range of interest. The stress dependency of the electromechanical coupling coefficient is enhanced. As a consequence, in order to achieve high yield figures on each wafer, advanced plasma shaping techniques are necessary. At Evatec we have flexible solutions (from large target diameters to DC+RF technology) to precisely adjust the plasma distribution over the wafer surface. These techniques allow us to reach stress distribution over the wafer surface less than ±50 MPa up to 5mm edge exclusion and well within the range required for application in high performance RF applications. With larger target size setup the excellent stress range is coupled with superior thickness uniformity of less than 0.15% (1σ).

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THE DOCTOR IS INSIDE YOUR BODY

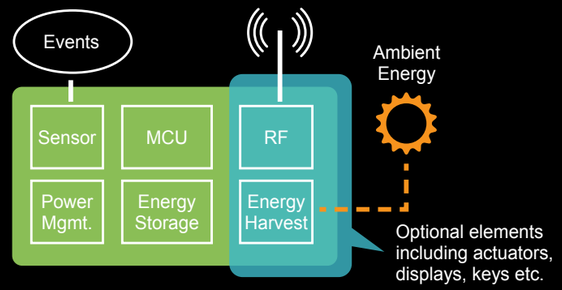
New technologies are emerging that will enable MedTech designers to create implantable sensing and therapeutic devices at mm-scale. Today's device sizes are typically defined by the largest component, the battery. Whilst cm-scale solid state batteries already exist for high end industrial and wearable products, medical device designers will soon be able to deploy them at mm-scale in the body due to advances in medical radio, in-body energy harvesting and secondary battery charging techniques. **John Tinson** from Ilika tells us how their thin film battery technology is now enabling true mm-scale IoT implantables.

The time has come

Until recently it seemed as if thin film solid state storage devices were a solution looking for a problem. Such batteries are created using semiconductor production techniques, cathodes, electrolytes and anodes of 10's of µm thickness are deposited onto a carrier layer such as a 6 inch wafer. Thinning and dicing the wafer then results in discrete cells, about 150µm thick, which can be stacked to form batteries. A 0.06cm^3 volume battery can store about 1mAh.

So many production steps on expensive and sophisticated equipment have placed the technology into a high value, low volume, industrial category until now. Today's applications are based around the current high temperature capability (to 150°C), or the sub 1mm z dimension of the thin film battery. Thin film solid state technology also supports high charge and discharge rates (C=>10) allowing a 0.3mA battery to drive the transmit and receive on a blue tooth radio device and so be part of an industrial sensing solution. If coupled to an energy harvester this opens the door to remote condition monitoring over long time periods taking advantage of the technology's high cycle count.

All that looks like it's about to change. The emergence of applications requiring tens of thousands of devices in the medical sector able to absorb a high initial price point, combined with further development towards higher energy densities, the deployment of high capacity and high accuracy manufacturing equipment plus long term reliability look set to move thin film solid state batteries more into the mainstream of battery applications.



Grabbing the opportunity

So far the technology was developed by SME's or research focussed technology centres, both lacking either the strategic intent or access to capital to move the technology into the medical arena. Ilika is a listed company (AIM) supported by institutions and investors proven over the years to take the long-term strategic viewpoint. By 2020 our analysis showed us that the time had come to invest across all the critical factor areas with a view to becoming a volume manufacturer of thin film solid state batteries. Money was raised, equipment orders placed and we are now well on our way to grabbing the opportunities such new markets will bring with cost-effective manufacturing technology.

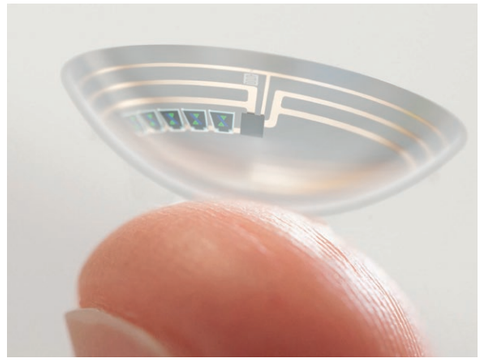
Sitting alongside this new technology are important breakthroughs in low energy ultrasonic radio, in-body-battery charging and energy harvesting which will influence designers. A new generation of medical start-ups is emerging, perhaps best described under the banner of Cyber-Physical Human Systems. In more layman's terms, this means an interconnected array of sensing and therapy delivering devices created at mm-scale and placed around the body, much nearer to the point of therapy delivery, capable of staying in the body for many years.

Applications

Many will have heard of the Opioids crisis in the USA when painkillers were over subscribed leading to addictions and many deaths. An alternative therapy via implanted devices sending a blocking signal to the nerve does exist but deployment has been limited. Smaller implants requiring simpler surgical procedures are seen as critical. Research also continues to uncover a wider array of therapies based around the stimulation of nerves aimed at seizures, sleep apnea and migraines to name but a few.

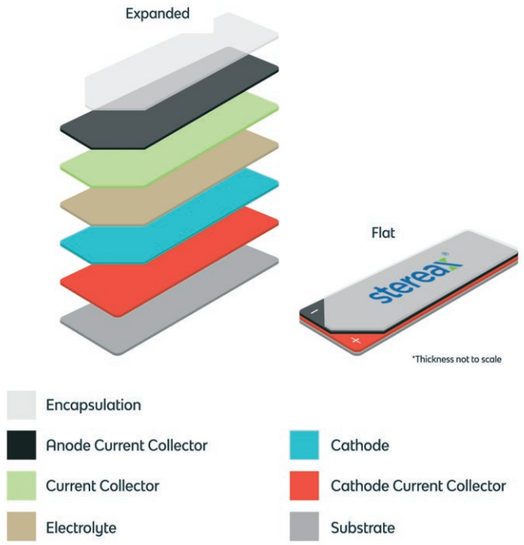
Communication enabled sensing applications include blood pressure, heart rhythm and glaucoma. All these, along with the need to satisfy patient adherence to medicine regimes that are crying out for smaller, less obtrusive and easier to install solutions. In the field of orthopaedics, such as a hip or knee implants, real time data on patient adherence to physio routines will be a great aid to better outcomes.

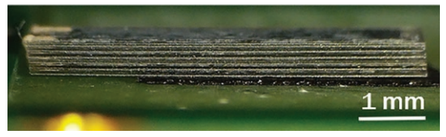
Whilst for the above applications a mm-scale energy storage device allows a significant improvement in device design there are some applications that will simply not be possible without ultra thin and mm-scale battery technology. There are at least ten companies around the world, some very well known, who are working on smart contact lens products with either a medical or AR/VR focus. Further out, continuous improvements in the performance of solid-state batteries may open up applications in implanted hearables such as inner ear placed active cochlear devices.

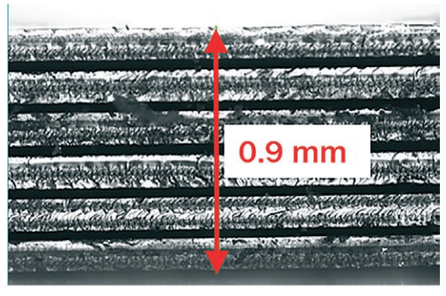


The technology

The production of our "Stereax" solid state, thin film battery takes place on a 6" glass wafer, used as a non-functional substrate. Initial depositions are for the first current collector which is sputtered and then the cathode deposited via thermal evaporation. The thickness of this layer will determine the amount of lithium available for transport and therefore the capacity of the battery. Deposition of the electrolyte, anode, the second current collector and primary encapsulation (insulation) layers takes place in our LLS EVO II sputter system which is ideal for our purposes with 5 sputter targets and a capacity of 12 wafers. It enables multiple production steps without breaking vacuum. The high uniformity, crack free layers at the volumes offered by the LLS are a critical factor in achieving the unit costs we need. Following the addition of a secondary encapsulant, the completed wafers are quality tested and passed to a set of thinning and dicing processes. The substrate layer is thinned to below 100µm and the individual batteries diced from the wafer. At this stage we have a battery cell 150µm thick which can be used alone as an ultra-thin battery, or it can be stacked to make higher capacity devices as shown below. Additional optimization of the deposition and thinning processes over the next year is set to take energy densities of the resulting battery to 200wh/l and beyond.







What's next

There's still a lot to be done by ourselves, our customers, and in the other supporting technologies required. Implanted devices are subject to very strict FDA accreditations which rely on data sets from thousands of hours and hundreds of samples. Novel therapeutic devices can typically take 3-5 years to reach market at a cost of ten's of millions of dollars, but the benefits to us all as individuals, and in cost savings to insurance and health services are great. We are excited at Ilika and look forward to working together with supplier partners such as Evatec at the start of a journey that is set to shape all our lives over the next ten years.

About the author

John Tinson

With a Physics degree from Birmingham University John's 30 year career in sales and marketing has spanned a range of industries; photonics, lasers, semiconductors and currently battery technology. Combining this background in industrial sales with his experience in strategic marketing of emerging technologies at early stage companies, makes his position at Ilika plc since 2019 a natural fit.

About Ilika

Ilika Technologies Ltd was founded in 2004 as a spin-out from the School of Chemistry at the University of Southampton. The company quickly established an international reputation for the rapid development of novel materials and secured commercial partnerships with a portfolio of blue-chip companies including Asahi Kasei, Shell, Applied Materials, Toyota and Murata. In 2014, Ilika started designing the Stereax family of solid state batteries and is now solely focused on the development and manufacture of solid state batteries for MedTech, IoT, Electric Vehicles and Consumer Electronics.

For more information about Ilika visit:
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Data and materials for all figures in this article have been kindly provided by the author.

OPTICAL WAVEGUIDE MATERIALS FOR HEAT-ASSISTED MAGNETIC RECORDING (HAMR)

Increasing the capacity of mainstream data storage devices is crucial to supporting the continued growth of the worldwide datasphere. With the shift to "cloud" storage as the preferred medium, the adoption of very high capacity hard drives requires drive makers to keep pace by increasing the storage density of recorded information on disc surfaces. Seagate's **Dr. Xiaoyue P. Huang** and **Dr. Michael C. Kautzky** explain how thin film technology has helped pioneer the introduction of new drive technology, Heat-Assisted Magnetic Recording (HAMR), to provide a commercially viable path beyond the density limits of today's perpendicular magnetic recording.

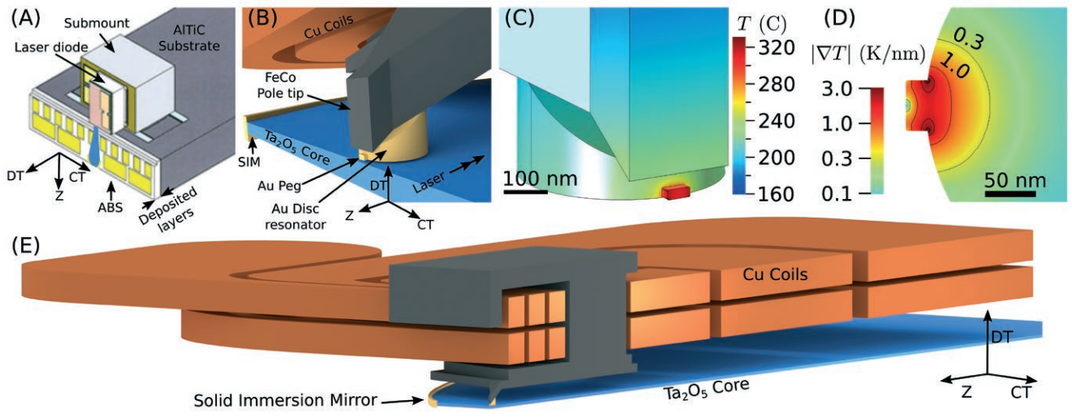

Figure 1: Overview of a HAMR Writer. (A) Recording head at 30X magnification. Approximate dimensions are 1.2 mm Down Track (DT), 700 um Cross Track (CT) and 100um in z. Note the direction of the waveguide core (blue). Media moves under the head in the +DT direction. (B) Zoomed version (30KX) of the head showing the near field transducer (gold), magnetic pole tip (gray), copper coils (orange) and tantala core (blue). (C) Temperature of the Near Field Transducer and Pole given an input power of 15mW (assuming 100% efficiency for the laser and light delivery system). (D) Cross section of the NFT showing the in-plane thermal gradients (E) Cross section through writer core, coils, NFT and solid immersion mirror (SIM).

To adapt to HAMR-specific data writing, recording heads in the drive are modified to be able to deliver thermal and magnetic spots <30nm to the media surface, and to modulate this process at data rates exceeding 1 Terabit/second. This is achieved by integrating a solid state laser, a thin film optical waveguide and a new nanofocusing near-field transducer ("NFT") into the head (Figure 1). During recording, near-IR laser light from the back of the head is collected by an optical input coupler and propagated down the waveguide where it is focused to illuminate the NFT. The incident light energy is converted into oscillations of surface free electrons in the NFT metals (called "plasmons"), and the associated electric field is then focused with a disc-facing antenna to heat the high-coercivity FePt recording layer above its Curie temperature. Using the magnetic field from a high-moment write pole in very close proximity to this heated spot, magnetic transitions are recorded and "frozen in" to the media layer during cool down, providing high recording densities with excellent thermal stability (Figure 2).

"Critical to the success of the new head components is their ability to meet both drive performance and reliability specs simultaneously"

Critical to the success of the new head components is their ability to meet both drive performance and reliability specs simultaneously (e.g. capacity, data rate, and cumulative failure rates of <1% at average data writing workloads over a 5-year period).

A major challenge here is that the operating conditions of the HAMR head during recording are extreme: >300°C peak temperatures, power densities in the NFT of ~150 TW/m^2 (which is ~25X higher than the sun), thermal gradients >1K/nm, pressures >10 atm (similar to a locomotive steam boiler) and an oxidative environment. Many conventional recording head materials fail under these conditions through a wide range of diffusion, phase change, chemical reaction and stress-related mechanisms. Indeed, initial HAMR head lifetimes were in the ms range due to poor durability. However, we have now addressed this through development of new thermally stable functional thin film materials across multiple functions. Examples include oxides for low loss optical transmission (which are the focus of this article), new transition metal alloys with engineered microstructure for efficient field confinement and high thermal conductivity, adhesion promoters for metal-dielectric interfaces, hard mask materials for sub-40nm nanoscale patterning and new diffusion barrier/heat sinking materials. These material innovations, together with improvements in design efficiency, downstream machining and test control, have enabled us to mitigate the HAMR-specific failure modes and increase mean HAMR head lifetimes from milliseconds to hundreds of hours, enabling launch of the industry's first HAMR 20TB drive.

During HAMR operation, the laser light needs to be carried from diode to NFT through a waveguide structure which is composed of a core and surrounding claddings. High-quality optical waveguide materials with low propagation loss are required to minimize the laser power required and avoid undue internal heating. Reactive PVD is the

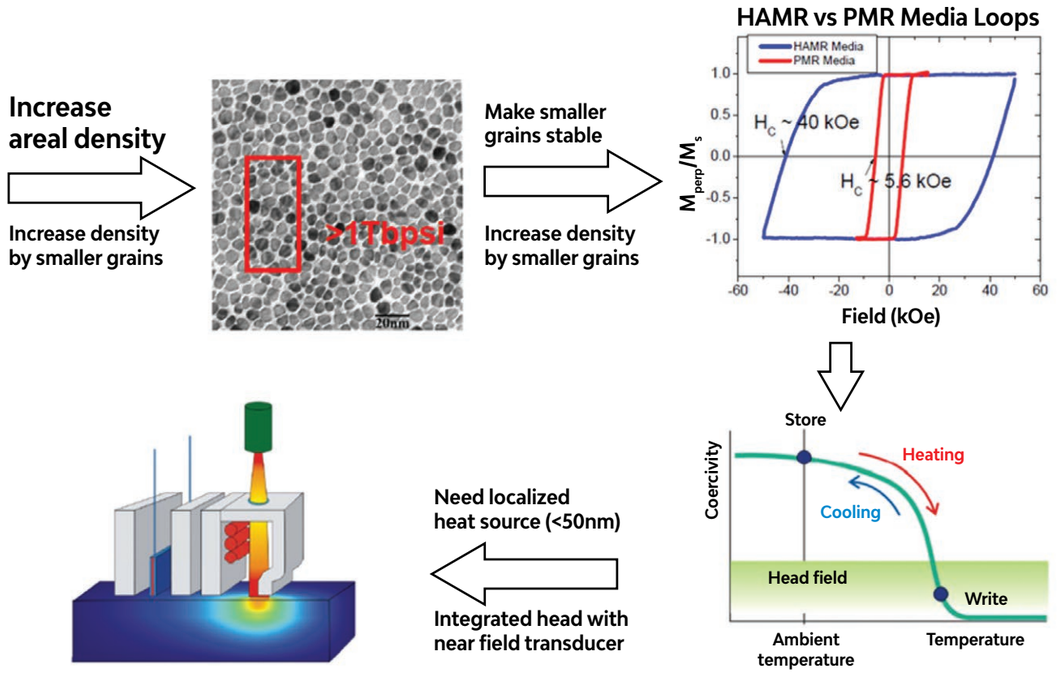

Figure 2: HAMR Recording Process.

favored technique to achieve this, providing high density amorphous films at reasonable deposition rates and low impurities at temperatures below 300°C (needed to avoid damage to the read sensor). For optical core layers, materials with index n > 2 are desirable for light confinement. HAMR development has focused on metal oxides, specifically d-band oxides such as Ta_2O_5 (n~2.1) which deposit in an amorphous state but with crystallization temperatures that typically exceed 800°C, reducing the risk for irreversible propagation loss increase

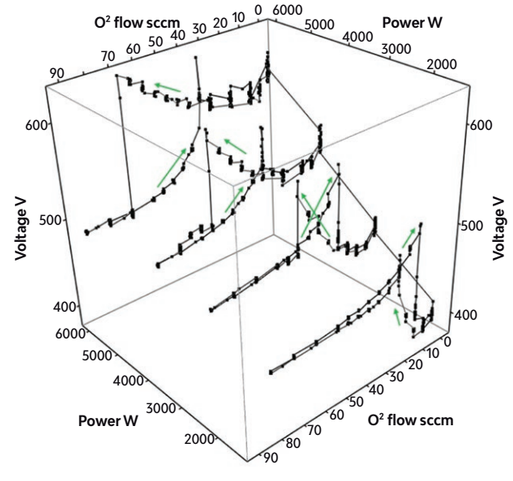

Figure 4: Hysteresis in r-PVD Ta_2O_5 at 200°C.

during service life of the head. Other oxides such as TiO_2 were also explored because of the high refractive index (n > 2.3) increasing the optical delivery efficiency. Such oxides also present the best resistance to chemical attack from wafer-level patterning and to ABS reaction during operation.

Robust waveguide core films are readily produced on Evatec's CLUSTERLINE® 200 PVD platform (Figure 3).

The reactive hysteresis map of a Ta_2O_5 process is shown in figure 4. As the cathode power increases, voltage vs O_2 flow hysteresis flips the polarity (indicated by the green arrows). This flexibility provides a wide process window for balancing deposition rate, particle generation and material stoichiometry. Films with optical loss less than 1dB/cm and less than 1% within-wafer sigma of Ta_2O_5 at deposition rates > 100 Å/min can be achieved on 200mm wafers in DC sputtering module. Similar reaction behaviors are also found in other high-n refractive metal reactive process, e.g. Ti.

"Conditions inside the HAMR head are challenging – with power densities 25 times higher than the sun"

TiO_2 is another attractive high refractive index material candidate which has also been studied in this system. A high purity 300mm Ti target was used with pulsed DC power during reactive sputtering in an Ar:O_2 mix. The

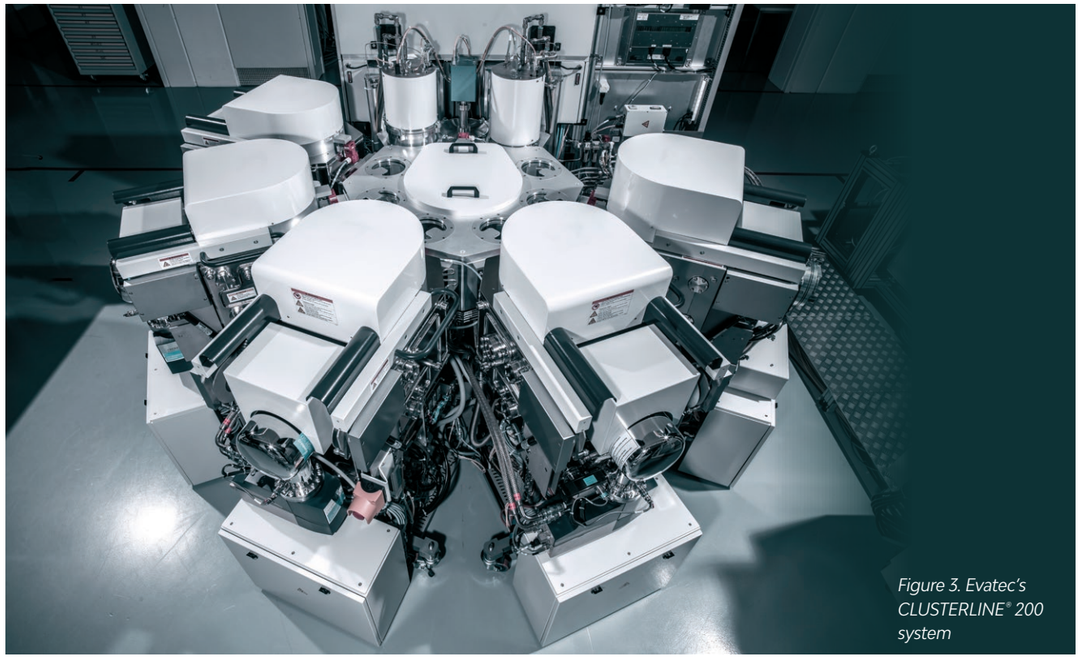

Figure 3. Evatec's CLUSTERLINE® 200 system

process was tuned to poison mode with sufficient O_2 flow in order to provide a stable and uniform low optical loss TiO_2 film on 200mm wafers (Figure 5)

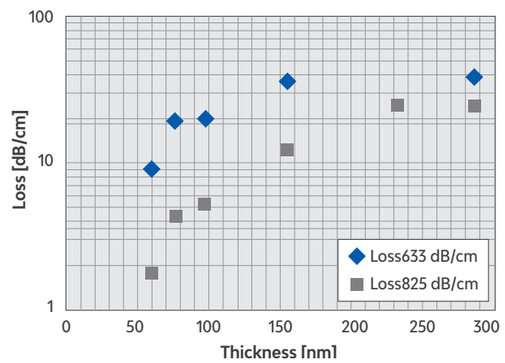

Figure 5: Optical propagation loss of r-PVD TiO_2 films.

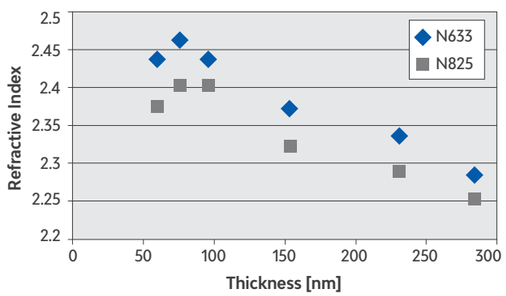

Figure 6: TiO_2 refractive index vs thickness.

At a substrate temperature of 200°C, the optical propagation loss of the sputtered TiO_2 films increased as the film thickness increased. This trend was the same for both 633nm and 825nm wavelengths, with losses below 40dB/cm and 25dB/cm respectively up to 285nm film thickness. Film index maxima over 2.4 were achieved between 50-100nm but declined to 2.25-2.3 at higher thicknesses (Figure 6).

The cross-section TEM images for a 143nm TiO_2 film revealed enlarged crystalline grain structure beyond ~54nm thickness when grown on amorphous SiO_2 substrates (Figure 7). The top part of the film also became more porous and rough with clear pinholes between grains. By contrast, the initial 50nm of TiO_2 film was more homogeneous. This deterioration of material quality at high thicknesses was consistent with the optical loss and refractive index trends.

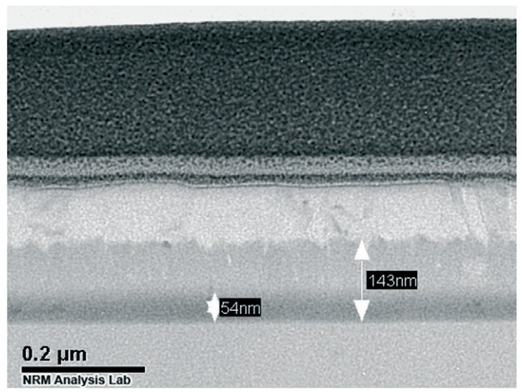

Figure 7: Cross-section TEM of r-PVD TiO_2 film.

To achieve high index TiO_2 films with low optical loss, composite layer films were developed (US Patent 8,681,595) by utilizing two process chambers in the CLUSTERLINE® system. The new TiO_2/Ta_2O_5 multi-layer films engineered very thin, sub-5nm Ta_2O_5 layers to break the crystalline growth of TiO_2 material. As shown in figure 8, the new film structure presented amorphous and uniform morphology.

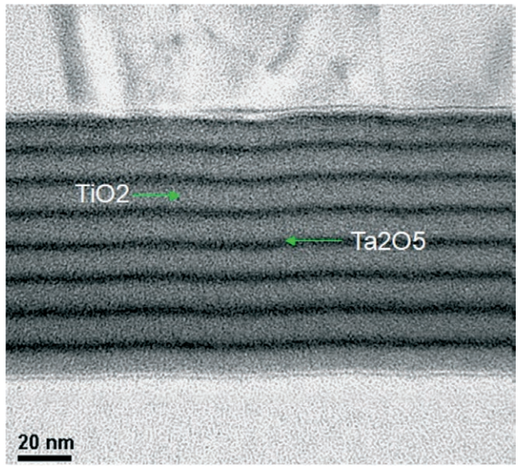

Figure 8: Multilayer TiO_2/Ta_2O_5 films with fully amorphous structure.

The composite layer films exhibited over tenfold lower optical waveguide losses (Figure 9), which are below 2dB/cm at 633nm and 825nm wavelengths. In addition, the refractive indices of multilayer films maintained n > 2.30 for all thicknesses, making them viable as an ultra-high index core material candidate.

Well controlled reactive sputtering processes have shown themselves capable of producing the high quality films of high-index oxide materials required for HAMR recording head waveguides.

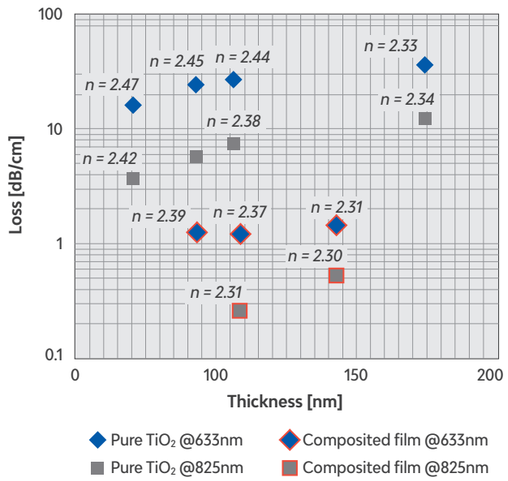

Figure 9: Optical loss and refractive index vs thickness for multilayer TiO_2/Ta_2O_5 films.

About the authors

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Technologies for e-mode GaN HFET front-end metallization

Gallium Nitride (GaN) is widely considered to have tremendous potential for wireless communication and power applications mostly in the form of RF power amplifiers and power switching devices, both of which are realized as heterojunction field-effect transistors (HFET). At the heart of any transistor and of a HFET in particular, lies the gate, source and drain metallization. These metal-semiconductor contacts are critically important for the functioning and efficiency of the device. Evatec Scientist **Dr. Clemens Nyffeler** explains what makes GaN based transistors so promising and the challenges that must be satisfied for the material to fulfil its potential in terms of both process technology and metrology techniques.

The Advantage of GaN

Wide band gap (WBG) materials have a compelling advantage over traditional Si-based devices such as the MOSFET or IGBT, especially for power applications. One of the reasons is that a material's band gap E_g is closely related to its breakdown electric field. A WBG transistor can sustain much higher voltages compared to a silicon-based transistor of the same size.

Silicon carbide (SiC) and gallium nitride (GaN) are both WBG materials with similar E_g of approximately 3.3eV and 3.4eV, respectively, and a breakdown field E_c of the order of 3MV/cm, roughly ten times larger compared to Si. This means that devices made from SiC or GaN can be made much smaller compared to a conventional Si power transistors with the same voltage rating. Since smaller structures have inherently smaller parasitic capacitances and resistances, such devices can operate with lower losses (smaller on-resistance R_{on}) and at higher frequencies (higher f_T).

In addition to having a large band gap, GaN also shows particularly high electron density n_s, mobility μ and saturation velocity v_{sat}, all of which further boosts its appeal. Independently of specific device design and dimensions, the suitability of a material for certain applications is described by several figures of merit (FOM), as illustrated in figure 1. In these figures, GaN clearly outperforms both Si and SiC, making it the ideal material, where both high power and high frequency operation or high-efficiency switching is required. An exception is Keyes' FOM, which is greater in SiC due to its high thermal conductivity, and the reason why SiC is preferred where heat dissipation is an issue.

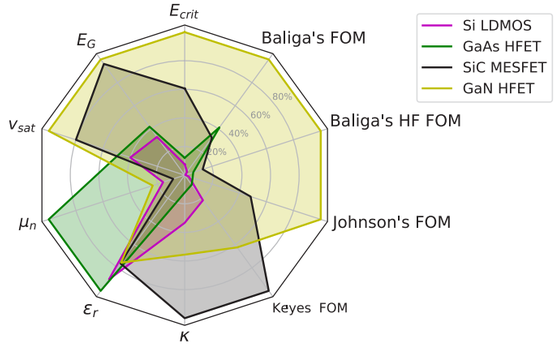
Figures of Merit

Baliga's
conduction losses due to *Ron* $\varepsilon_s \mu E_g^3$

Baliga's
for high frequency μE_c^2

Johnson's
power handling at high frequencies $\upsilon_{sat} E_c / 2\pi$

Keye's
thermal limitaions to switching $\kappa \sqrt{\frac{c\,\upsilon_{sat}}{4\pi\varepsilon_s}}$



Material Property	Symbol	Si	GaAs	SiC	SiC
Critical (breakdown) electric field	E_c [V / m]	0.3	0.4	2.0	3.3
Energy band gap	E_g [eV]	1.1	1.4	3.3	3.4
Electron saturation velocity	V_{sat} [10^7 / cm s]	1.0	1.2	2.0	2.5
Electron mobility	μ_n [cm^2 / V s]	1350	8500	720	2000
Relative permittivity	E_r [1]	11.8	13.1	10.0	9.9
Thermal conductivity	K [W / cm K]	1.5	0.6	4.5	2.5

Figure 1: Figures of merit comparison between semiconductors materials. Interestingly, while GaAs shows very high electron mobility, this does not translate into an advantage due to the relatively low values of other material properties. In contrast, the favorable values across the board for GaN allow it to dominate the FOM spectrum with only one exception. Data from reference [1].

Devices built on GaN

GaN-based transistors are most often realized as heterojunction field effect transistors (HFET), in contrast to the metal-oxide-semiconductor FET (MOSFET) built from Si or SiC. These MOS structures, ubiquitous in Si electronics for over half a century, are in fact difficult to realize with III-V compound semiconductors.[1]

At the heart of the HFET lies a interface between two (hetero-) epitaxially grown layers such as AlGaAs on GaAs or AlGaN on GaN. Band bending at this heterojunction leads to the formation of a quantum well, in which a high-density so-called two-dimensional electron gas (2DEG) exists, as shown in figure 2. This 2DEG is the equivalent of the inversion layer in a MOSFET at the oxide-semiconductor interface, but with substantially enhanced electron mobility, which is why the HFET is also commonly called high-electron mobility transistor or HEMT.

Instead of a metal-oxide semiconductor stack, the gate of a GaN HFET consists of a Schottky junction, where the gate metal is in direct contact with the AlGaN layer. This junction insulates the gate from the channel, albeit not as well as the oxide in a MOS structure (efforts have also been directed towards creating hybrid MOS/HFET devices). For RF and power applications, however, a limited gate leakage is less of a concern compared to the strict requirements for highly integrated logic circuits.

A greater concern is that the HFET devices described above are "normally on" devices [2]. In contrast to a MOSFET, the GaN transistor channel is conducting when no gate bias voltage is applied (the potential V_G at the gate, referred to the source potential V_S is zero). Such devices are called depletion-mode (d-mode) transistors because a negative V_G is required to deplete electrons from the heterojunction and turn the device off.

One way of addressing this problem and create so-called enhancement-mode (e-mode) transistors is to add a p-doped GaN or AlGaN layer under the gate, shifting the conduction band upwards, so that the quantum well is lifted above the Fermi level (see figure 2b). Now a positive gate voltage, higher than a certain threshold voltage is needed to restore the 2DEG in the heterojunction and turn the device on, letting it behave just like a standard MOSFET. This improves device operation safety, in particular for power switching applications, and allows for simplified driver circuits.

Process Challenges

Sputter induced damage

A general concern when employing plasma-enabled processes on GaN surfaces, such as dry etching or sputter deposition, is the risk of incurring damage to the GaN crystal structure caused by highly energetic species originating from the plasma. In LED fabrication this manifests in reduced light output and an increased forward voltage. In HFET structures it can lead to reduced electron density of the 2DEG and higher R_{on}. Therefore, it is important to reduce or eliminate the ion bombardment with dedicated process technology and careful tuning of process parameters.

Evatec has a long track record of enabling the critically important damage free deposition of metals and transparent conductive oxides (TCO) such as ITO, IZO and GZO on sensitive materials including GaN and GaAs. CLUSTERLINE® 200 Batch Process Systems have been instrumental in driving high volume GaN LED production with the highest requirements in damage control and device efficiency, employing high throughput PVD systems with combined RF+DC sputter deposition.

On the CLUSTERLINE® 200 Single Process Module (SPM) platform, the options for low-damage sputter deposition include the 300mm RF+DC source for high throughput as well as our facing-target cathode (FTC) technology for ultra-low damage at reduced throughput. These technologies work best in a complementary fashion: two FTC sources are paired in an MSQ single process module with two 100mm RF/DC circular sources, which can be switched on after an initial damage free layer is deposited by the FTC. This may be followed by transfer to a 300mm target module for high-rate deposition of the bulk material for thick films.

The effect of damage is often determined indirectly by building devices such as LEDs and transistors and measuring their characteristics V_f and R_{on}, respectively. Raman and Photoluminescence spectroscopy, on the other hand, are measurement techniques allowing for a direct assessment of the GaN crystal quality and enable us to develop and verify our damage free processes without relying on device manufacturing capabilities. Both techniques are non-invasive: the substrate is illuminated by a light source and the light emitted from defects and band-gap recombination (PL) or the light emitted by crystal vibrations (Raman) is recorded.

1 The reason is that III-V compounds do not allow to grow the same high-quality oxides with a clean oxide-semiconductor interface that can be realized with Si and SiO_2, which is crucial for MOSFET operation.

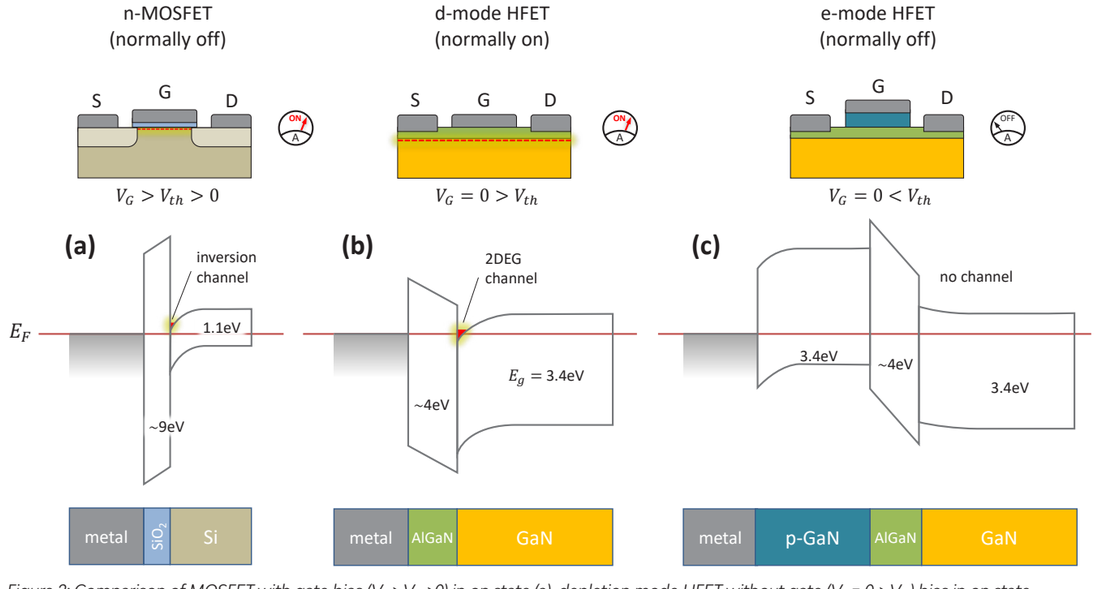


Figure 2: Comparison of MOSFET with gate bias ($V_G > V_{th} > 0$) in on state (a), depletion mode HFET without gate ($V_G = 0 > V_{th}$) bias in on state (b) and enhancement mode HFET without gate bias ($V_G = 0 < V_{th}$) in off state (c). At the top: schematic cross section of simplified device, middle: band diagram sketch along a vertical line across gate, channel and bulk of the device, bottom: index of materials in the band diagram. The inversion layer and 2DEG in the MOSFET and HFET in (a) and (b), respectively are indicated in red. Note that typically the GaN layer is unintentionally n-doped, leading to a conduction band close to the fermi level E_F. An example of band simulation can be found in reference [3].

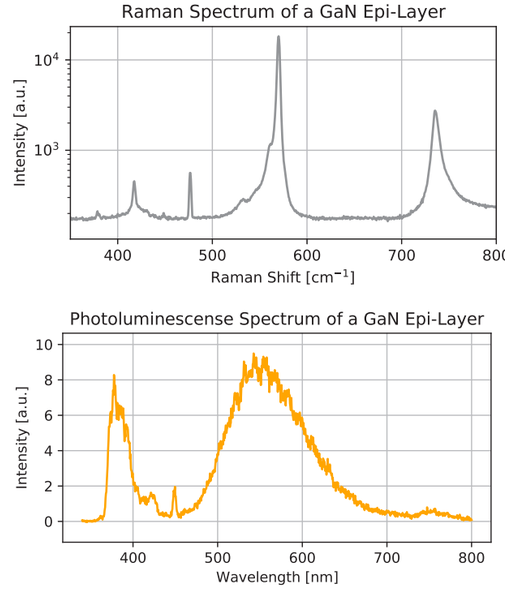


Figure 3: Example of a typical Photoluminescence (left) and Raman Shift (right) Spectra of an unprocessed MOCVD grown GaN epi-Layer, purchased from a commercial supplier. The PL spectrum (left) indicates a near band photon emission around 366 nm, and defect-related bands at higher wavelengths. Particularly, the intense and broad emission band centered around 550 nm is related to point defects [4]. Courtesy of Dr. F. Pezzoli from the Università degli studi di Milano Bicocca, Italy. The Raman spectrum (right) consist of two main phonon peaks: E_2 (high) and A_1 LO around 570 cm^{-1} and 735 cm^{-1}, respectively. Their spectral position and width strongly depend on the GaN stress and crystal quality.

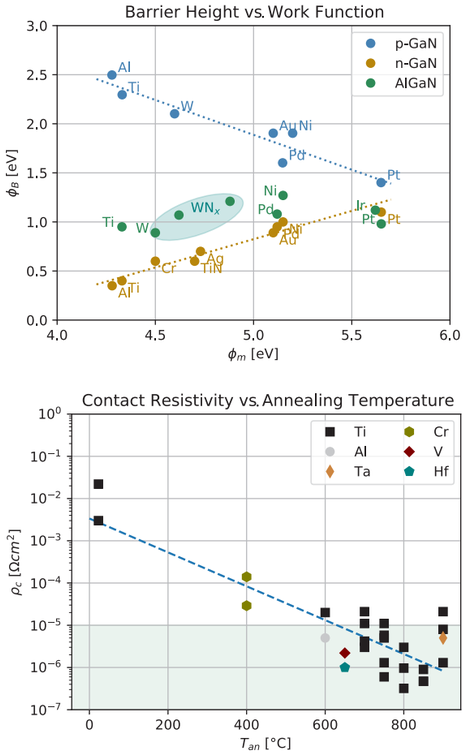


Figure 4: (a) Schottky barrier height for various metals when contacting n-GaN and p-GaN and AlGaN/GaN heterostructures. A low barrier height is needed for ohmic contacts and larger barrier height for gate metallization. The dashed lines are a guide to the eye. (b) Contact resistivity of various metals when contacting n-GaN as a function of annealing temperature. The shaded area represents the desirable range of resistivities. Both figures are adapted from reference [5], additional data from refs [6] [7] [8] [9].

Source and Drain Metallization

Source and drain must be ohmic contacts with least possible contact resistivity to minimize the series resistance adding to R_{on}. Therefore, the contact material needs to have low workfunction $Ø_m$ < 4.5eV when contacting an n-type GaN to keep a low Schottky barrier height at the metal-semiconductor junction. The opposite is true when contacting p-GaN and a similar but a less pronounced trend manifests for AlGaN/GaN heterostructures (Figure 4). The multilayer systems typically used for metallization start with a refractory metal (Ti, Ta, Hf) as a contact layer, followed by a thicker Al overlayer and a capping layer, such as Au, W or TiN, preventing surface oxidation.

After the metal stack deposition, a high temperature annealing is typically performed to reach the required low contact resistivity of the order of p_c <10μΩcm². The temperatures for this anneal are in the range from 600°C to 900°C, while the ambient environment must be carefully controlled to prevent oxidation. One of the mechanisms to improve the contact resistance is an effect where nitrogen is extracted from GaN to form TiN at the Ti/GaN interface. The benefit is due to a further reduced barrier and an increased n-type doping due to donor-like behavior of nitrogen vacancies in GaN [5].

Our heater solution offers an efficient option for in-situ contact metal annealing, allowing for temperatures up to 860°C (Si Substrates) or 800°C (Sapphire) via radiative heat transfer under high vacuum with the help of in-situ pyrometer wafer temperature monitoring. It is available either as a dedicated annealing module or as part of a process module for high temperature sputter processes.

Gate Metallization

Compared to source and drain, the gate metallization contact layer is subject to different requirements. The junction formed with the underlying GaN layer should prevent any current flowing through the gate during normal operation of the transistor. To minimize such gate leakage, the Schottky barrier height $Ø_B$ must be as large as possible and a reaction with GaN is undesired. Which material should be chosen depends on whether the gate metallization is deposited on n-type GaN or p-type GaN (for e-mode transistors), although the choice is less critical on p-GaN, which naturally forms larger barrier heights as illustrated in figure 4.

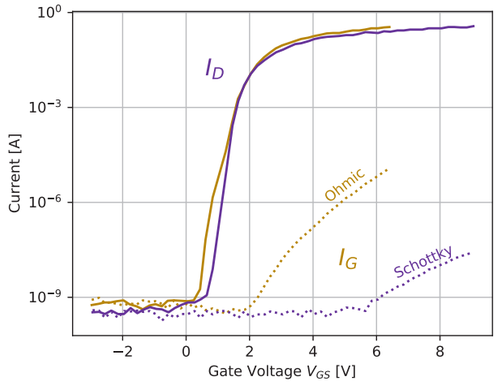


Figure 5: Drain current (desired, solid lines) and Gate current (undesired, dotted lines) for two devices, one with ohmic and the other with Schottky contact. Ideally, no gate current should be present. The Schottky contact device shows lower leakage currents and better gate voltage swing, i.e. larger range of gate voltages, where gate current remains low. Figure adapted from reference [6].

Refractive metal nitrides (TiN, WN, TaN etc.) are often used as gate contact materials. They show good conductivity (sometimes better than their metallic counterparts), and are chemically inert and therefore less reactive with GaN. In addition, they tend to form good diffusion barriers. Relevant properties like conductivity and composition can be tuned during reactive sputter deposition using parameters like gas flow and power.

The work function $Ø_m$ as the most important property for ensuring an effective Schottky barrier, may depend both on the nitrogen content and the microstructure of the film. It is therefore important to measure the work function directly with a suitable method. This is possible using a scanning probe microscope (SPM) equipped with Kelvin probe functionality that can measure the film's surface potential allowing deduction of its work function. This method, however, is extremely sensitive to sub-monolayer surface contaminations. A more reliable method, able to produce absolute values of $Ø_m$, is to use photo-electron spectroscopy with a UV-light (UPS) or an X-ray source (XPS). Here the work function is obtained by measuring the electron's kinetic energy after emission from the material due to excitation by a UV or X-ray photon. This kinetic energy equals the known photon energy minus the energy required to escape from the material, which is the definition of $Ø_m$.

The electrical resistivity may also be of interest as an intrinsic property or its variation as an indicator of process stability and within wafer uniformity. An effective technique for its determination is a combination of 4-point probe sheet resistance measurement and X-ray reflectometry (XRR). The latter is an exceptionally precise and robust way for film thickness measurement, both for transparent and opaque films including metals, and also provides information about the materials density.

Diffusion Barriers

Another potential cause of gate leakage is the diffusion of highly mobile metal species from the conductor layer on top such as Al or Cu. Migration through the contact layer and into the GaN can lead to current paths shorting the gate with the 2DEG. To prevent this, the contact layer must also act as an effective diffusion barrier. This, again, makes the family of conducting transition metal nitrides particularly suitable for the task.

For a contact metal nitride to be effective as a barrier layer, its composition and microstructure must be well controlled. Material properties including electrical conductivity, work function and microstructure strongly depend on the nitrogen content in the film. In the case of TiN, where resistivity reaches its minimum value, a stoichiometric film composition is often desired. Achieving stable process conditions in this case requires advanced process control technology as implemented in Evatec's deposition modules.

In some cases, however, the best barrier performance is obtained at non-stoichiometric composition. In WNx for example, a nitrogen content of about 20 at% leads to a favorable mixture of phases containing W2N grains and elemental W [7]. Whichever the material, a highly dense and amorphous microstructure is generally desirable as opposed to a polycrystalline material, where diffusion is facilitated along grain boundaries.

A versatile tool for thin film characterization, X-ray-diffractometry (XRD) is routinely used to identify material phases, detect crystal orientation, perform grain size estimation and more. Complemented with atomic force microscopy and scanning electron microscopy, a comprehensive range of techniques for the analysis of thin film microstructure is at hand. Where material composition is of interest, we rely on EDX, XPS and RBS/ERDA. While EDX is a fast and uncomplicated method well suited for metal alloys, it falls short where high precision and/or the detection of light elements is required. While these limitations are overcome when employing XPS, a wealth of additional information can be accessed with this technique, including the analysis of chemical states and sputter depth profiles.

Here to support customers

As with most applications, a solid understanding of the material requirements, whether intended as a diffusion barrier, an ohmic contact or a Schottky barrier, is essential. We are here to provide and develop the optimal processes for customers considering the electrical, mechanical, and structural properties needed for each particular layer in the GaN HEMT manufacturing process. First and foremost, this means undertstanding their material and layer requirements. Suitable combinations among the portfolio of Evatec's process technologies can then be selected for the specific challenges at hand. The final element is knowing which material properties to examine and which measurement technique to employ to ensure the process produces the right results.

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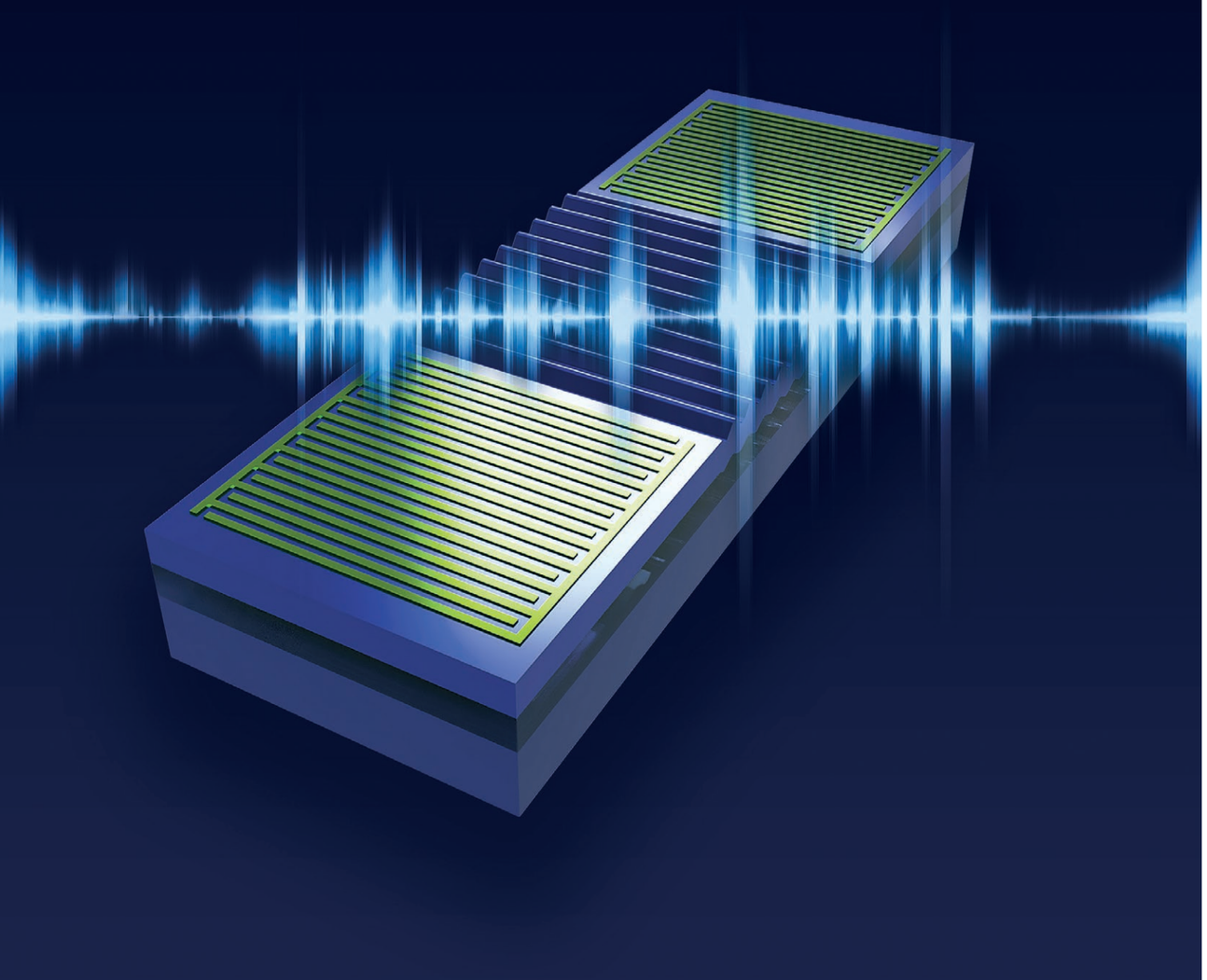
Ready to innovate for future wireless systems

For several decades, micro-acoustic devices based on surface acoustic waves (SAW) have played a key role in the development of wireless digital communication systems. Evatec's Principal Scientist **Dr. Claudiu Valentin Falub** shows why Thin Film SAW is a game changing technology for the latest fourth generation (4G) and the upcoming fifth generation (5G) cellular networks, and why Evatec is your ideal partner for the high volume manufacturing of these novel RF components.



Technology Generation	1G	2G	3G	4G	5G
Period	1980 – 1990	1990 – 2000	2000 – 2010	2010 – 2020	2020 – 2030
Frequency	150MHz / 900MHz	900MHz / 1.9GHz	1.8 – 2.5GHz	2 – 8GHz	3 – 300GHz
Bandwidth	Analog	25MHz	100MHz	100MHz	100x BW per unit area
Data rate	3kbps	64 kbps	164kbps – 2Mbps	50 Mbps – 1 Gbps	> 10Gbps

Figure 1: Evolution of the wireless phone technology since 1980, with a new generation emerging approximately every 10 years.

Wireless connectivity evolution towards 5G and beyond

Communication in one form or another has been a fundamental need of humanity since the dawn of history, but the giant leap that radically changed how we communicate and interact with each other and with the surrounding world has only been enabled in the last few decades by revolutionary advances in broadband radio-frequency (RF) networks and mobile devices.

In the meantime, wireless connectivity has evolved tremendously [1] (see also figure 1 for a summary of the evolving wireless technologies), but we are still in the early stages of "anything-anywhere-anytime" paradigm shift, which is today's vision for the communication network of the future. Transition from Person-to-Person (P2P) to Machine-to-Machine (M2M), Vehicle-to-Infrastructure (V2I) and Internet-of-Things (IoT) communications is going to require huge improvements in network data transfer rates, approaching the upper limits for wireless transmission predicted by Shannon's "noisy-channel coding" Law [2], which can only be enabled by improved band selection filters and multiplexers in the RF front-end modules (RFFEM) of the wireless systems. These requirements challenge the manufacturers to explore novel designs, material systems and fabrication techniques, and packaging and integration technologies.

Advance today's RF filters for tomorrow

RF filters are devices used in both the transmitter and receiver of communicating terminals, composed of several resonators connected in a ladder-like network, which allow the passage of signals of certain frequency bands. Since the 4G low-band (<1GHz) and 4G mid-band (1-2.6GHz) have become very crammed (i.e. presently, there are more than 30 frequency bands allocated to the 4G network

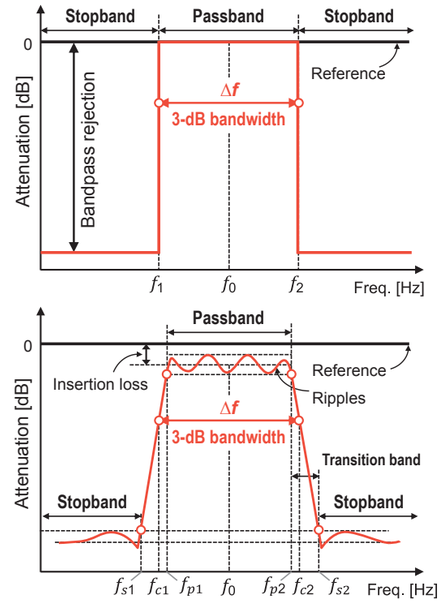


Figure 2: Typical frequency response for ideal bandpass filter (top) and real bandpass filter (bottom), where f_0 and Δf are the central frequency and passband width (i.e. 3-dB bandwidth corresponding to the half-power attenuation and cutoff frequency f_c), and f_s and f_p are the stopband and passband edge frequencies, respectively.

technology and new ones continue to be allocated), the general trend of the RF filter requirement is a wider bandwidth (e.g. Δf) at a higher center frequency (f_0) with the lowest possible insertion loss and temperature-induced frequency drift, the highest quality factor (Q) and steepest passband skirts (Figure 2).

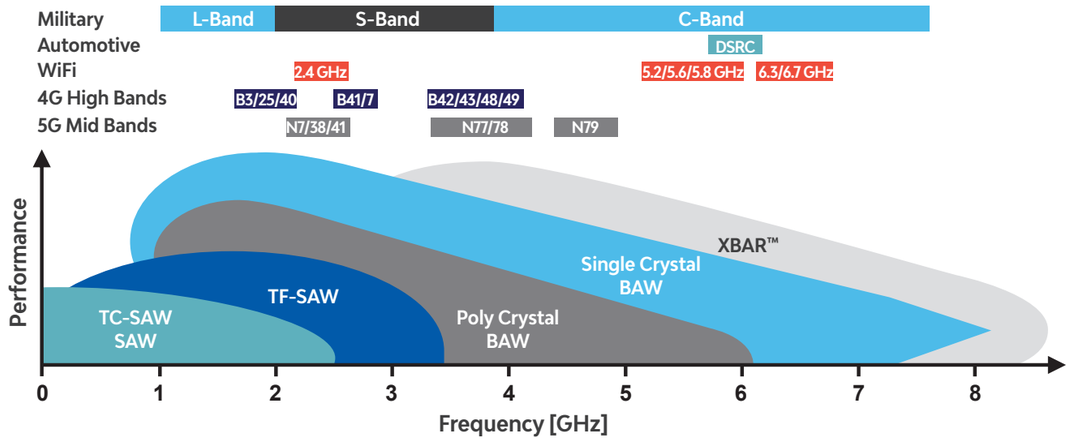


Figure 3: Market applications and band allocation of RF filters, where TC-SAW and TF-SAW denote the temperature compensated and thin film SAW technologies, respectively, XBAR™ is a trademark of Resonant Inc. representing the laterally excited BAR technology, and DSRC stands for "dedicated short range communications", a Vehicle-to-Infrastructure (V2I) wireless technology (adapted from [3]).

Moreover, there is a need for improved power handling and frequency coexistence filtering solutions in a cost effective compact package, especially since a modern multi-band mobile phone may contain up to 100 filters.

Among various existing RF filters, the micro-acoustic devices based on the complementary surface acoustic waves (SAW) and bulk acoustic waves (BAW) technologies are the only systems that cost effectively provide the required frequency selectivity for wireless data transmission with sufficiently small footprint for frequencies up to about 8GHz (Figure 3). For that reason, they are the dominant off-chip RF filters in mobile devices today, and component manufacturers ship billions of units per year.

Current and future challenges

The success of acoustic RF filters has always been an attribute of their design. Let's take for example the case of SAW filters, in which a pair of interdigitated transducers (IDTs) fabricated on well oriented piezoelectric crystal substrates, such as ST-quartz, 42° YX-cut lithium tantalite ($LiTaO_3$ or LT), or 128° YX-cut lithium niobate ($LiNbO_3$ or LN), etc., converts the electrical energy to mechanical acoustic waves and then back to electrical energy (Figure 4a). Remarkably, this reversible phenomenon enables signal processing of GHz electromagnetic waves into much smaller packages in view of the much slower (~10^5 times) propagation velocities of the acoustic waves!

There are, however, a few drawbacks to this approach. Thus, the lithographic and patterning resolution in fabricating the IDT metal fingers limits the high-end frequency of the SAW filters to about 3GHz before the dimensions of the transducers become inpractical (at these frequencies the tolerance required for the line width exceeds the required tolerance for CMOS metal processes!). Moreover, in view of the exceedingly small lateral structures, power handling capabilities of the SAW filters are also limited at high frequencies because of the very high current densities involved.

To tackle these difficulties and still be able to filter the higher frequencies, BAW technologies, such as the thin film bulk acoustic resonator (FBAR) and solid mounted resonator (SMR), came into play. In these devices, high density acoustic waves bounce between two metal electrodes that sandwich a piezoelectric layer, forming a standing acoustic wave with a resonant frequency that increases with the propagation velocity of the waves and the piezoelectric layer thickness.

While on the one hand BAW technologies should deliver superior performance with higher Q-factor and power handling, and lower insertion loss and temperature drift at higher frequencies, on the other hand their manufacturing is more challenging, and the process complexity and costs are high compared to SAW. Furthermore, BAW devices simply cannot compete with their SAW counterparts below 1.5GHz because of the larger size of the former at those lower frequencies (i.e. footprint area ~$1/f^2$, where f is the frequency). Consequently, to select between these two complementary acoustic technologies, one must balance the application frequency, performance and manufacturing costs.

The somewhat indefinite boundary between SAW and BAW applications lay previously at ~1GHz, but thanks to several improvements in SAW technology this boundary has been pushed in a first phase to around 2GHz. Thus, to improve the Q-factor and reduce the losses, the cut-angle of crystal substrate and the geometry and metallization ratio of IDT electrodes have been optimized. Moreover, the temperature induced frequency drifts characterized by the temperature coefficient of frequency (TCF) were

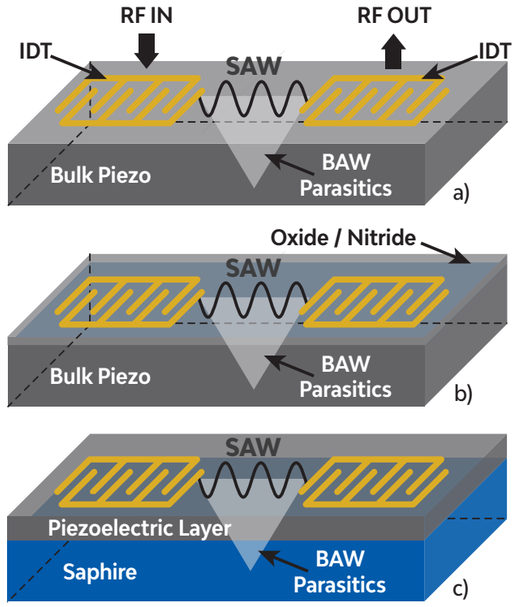


Figure 4: a) Standard SAW filter. b) Temperature-compensated SAW (TC-SAW) filter with overcoated IDTs; c) TC- SAW with thin piezoelectric layer bonded on a stiff substrate.

addressed by compensation methods for the temperature characteristics of the substrate materials, so called temperature compensated SAW (TC-SAW) technologies: i) dielectric overlay (e.g. SiO_2, SiOF, Si_3N_4, etc.) on the IDT (Figure 4b) [4], and ii) wafer bonding technologies (Figure 4c) [5].

While TC-SAW technology was an important milestone for acoustic RF filter manufacturers, the energy leaked into the substrate still hindered those devices from operating at their full potential.

A breakthrough technology

Major improvements with respect to the standard SAW and TC-SAW structures, such as a 4 times larger Q-factor, 80% reduction of TCF and 20% wider bandwidth, have recently been enabled by innovative thin film technologies [6,7]. The novel RF components, so called thin film SAW (TF-SAW) devices, exhibit comparable or better performance than their BAW counterparts with a lower cost up to around 3GHz [8]. As a result, all 4G mid-bands, most of the 4G high-bands and some 5G mid-bands can now be served by cost-competitive high-performance SAW filters (Figure 3).

Essentially, the main innovation brought by TF-SAW was the suppression of losses (e.g. bulk leaky waves, sideways radiation, diffraction effects) by means of thin film Bragg reflectors consisting of appropriate acoustic layers with alternating λ/4 thick low (e.g. SiO_2, SiON, Si_3N_4, etc.) and high (e.g. Al_2O_3, AlN, Ta_2O_5, etc.) acoustic impedance (Z) fabricated under a λ/2 thick piezoelectric crystal plate (Figure 5a).

This technology was first developed by Murata under the name "Incredible High-Performance SAW" or "I.H.P. SAW" (Figure 5b) [6,7], and the first RF filters were introduced to the market in 2019 in the Sony Xperia XA2 mobile phone as a WiFi 2.4GHz path between the transceiver and triplexer [8,9]. A simplified and optimized layer stack was finally chosen for the device manufacturing, without a high-Z layer towards the Si substrate, which exhibited virtually no performance loss with respect to more complex structures [10].

In the meantime, other manufacturers have begun to pursue and assert this new technology, such as Kyocera, Skyworks, Qorvo, Taiyo Yuden, and especially Qualcomm who introduced their own TF-SAW technology for the frequency range 0.6–2.7GHz, so called "ultraSAW" (Figure 6) [11]. In Qualcomm's approach the TCF compensation is performed by means of a two layer stack, a low-Z (SiO_2) thin film and a thin functional layer (FL) between the low Z

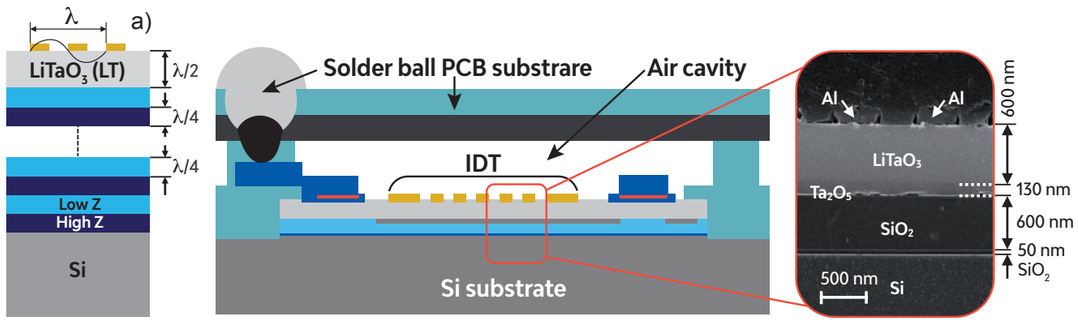


Figure 5: a) Basic concept of the thin film SAW (TF-SAW) technology. b) Die cross-section schematics of Murata I.H.P. SAW filter fabricated by surface micro-machining on 6" Si substrates, LT wafer bonding and polyimide protection using 9 lithography steps. The inset shows a cross-sectional TEM of the filter layer stack, consisting of a Ta_2O_5 (high-Z) layer and two SiO_2 (low-Z) layers deposited on the LT/Ta_2O_5 and Si wafers prior their bonding (adapted from Ref. [8]).

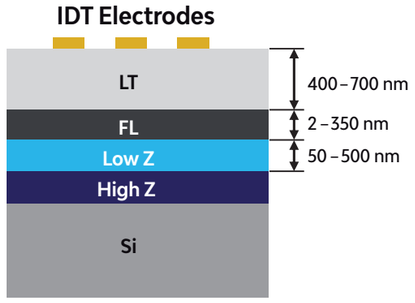


Figure 6: RF360 Qualcomm TF-SAW concept, where FL is a functional layer consisting of an ion-implanted LT layer devoid of piezoelectric properties, whereas the low-Z layer (e.g. SiO_2) and the optional high-Z (e.g. AlN) layer can be fabricated by PVD or CVD; adapted from Ref. [12].

layer and the thin piezoelectric plate [12]. The FL should have similar mechanical properties to those of the piezoelectric plate, but it should now exhibit piezoelectric properties, which can be achieved by means of ion implantation of the LT plate to a desired depth. Consequently, the thickness of the low-Z layer having poor acoustic properties can be reduced, which improves the acoustic properties of the whole layer system.

For the moment, TF-SAW devices (I.H.P. SAW, ultraSAW) will progressively be introduced in the 1.8–3GHz range, where BAW / FBAR components were previously more competitive, e.g. Band 25+66 Multiplexer, 2.4GHZ Wi-Fi, 4G-LTE high-bands (B25, B40, B41 and B7), and some 5G mid-bands below 3GHz (N7, N38 and N41). However, the question remains if TF-SAW technology would still be a viable cost-effective solution for the "Sub 6GHz" range, which was previously considered to be impossible for the conventional SAW devices, and promising results recently reported by Murata at 5GHz [13] would seem to suggest so, even though the standardization of 5G is currently ongoing.

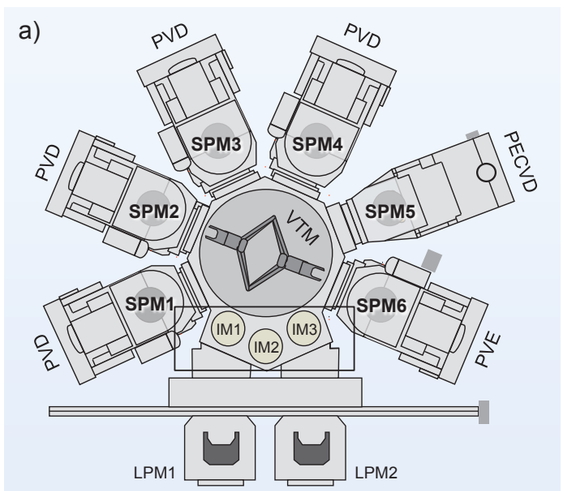
The new technology needs robust process solutions

To meet the more demanding technical requirements for TF-SAW device fabrication caused by the increased design complexity, manufacturers need to be able to produce high quality acoustic layer stacks, which fulfill the mechanical and physical property specifications with superior uniformity and repeatability cost-effectively. Thus, since the device fabrication process flow involves a wafer bonding step, besides tuning the thermo-elastic properties of the amorphous low-Z thin films (e.g. SiO_2, Al_2O_3, etc.) that act as TCF compensating layers one also needs to reduce their residual stresses for an improved bonding strength between the Si and piezoelectric wafers.

To keep up with higher production demands for these novel devices, Evatec solutions comprise a variety of tools for high volume manufacturing on 200mm wafers for not only the high performance acoustic dielectric layers (e.g. SiO_2, AlN, Ta_2O_5, etc.) below, but also the metallic IDT fingers (e.g. Al, W, Ti, etc.) above the piezoelectric thin plate:

- The newly released BAK 911 and BAK 941 for high-throughput evaporation of IDTs and ePAD structures also in lift-off configuration (see the focus article at page 90).
- The multi process technology cluster solution which comes in two different variants: CLUSTERLINE® 200 SPM and CLUSTERLINE® 200 BPM.

For ultimate flexibility CLUSTERLINE® 200 SPM is the ideal choice, as it can be equipped with up to six Physical Vapor Deposition (PVD) / Physical Vapor Etching (PVE) modules, or up to four Plasma Enhanced Chemical Vapor Deposition (PECVD) and two additional PVD / PVE modules (Figure 7a). In addition, this deposition system can be configured with two outgassing stations for pre-cleaning treatment and wafer pre-heating to process temperature, and two stations for cooling down the processed wafers.



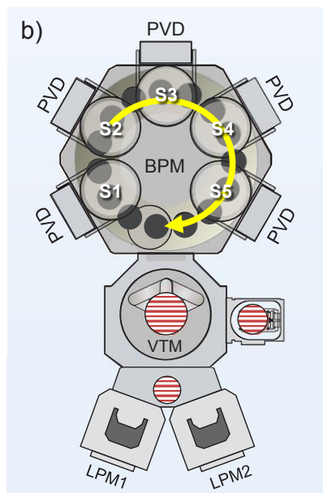


Figure 7: Evatec process solutions for high-volume manufacturing of TF-SAW devices: a) CLUSTERLINE® 200 II equipped with 6 single wafer process modules (SPM1 to SPM6), e.g. 4 PVD, 1 PECVD, 1 PVE, a central vacuum transfer module (VTM), 3 interface modules (IM1 to IM3), and dual loading port system (LPM1, LPM2); b) CLUSTERLINE® BPM equipped with a large turntable and 5 PVD stations (S1 to S5).

Film properties (6" / 150mm wafers)	CLUSTERLINE® 200 II			CLUSTERLINE® BPM	
	SiO_2	Ta_2O_5	AlN	SiO_2	Ta_2O_5
Film thickness	600nm ± 5	200nm ± 5	1000nm ± 5	600nm ± 5	500nm ± 5
Thickness uniforminty (within wafer) 1σ	≤ 1.0%	≤ 1.0%	≤ 0.3%	≤ 0.4%	≤ 0.3%
Thickness uniforminty (wafer to wafer) 1σ	≤ 0.3%	≤ 0.3%	≤ 0.3%	≤ 0.3%	≤ 0.3%
Depostion rate	≥ 0.50nm/s (2.5kw)	0.75nm/s (6 kw)	≥ 1.00nm/s (7.5 kw)	0.20*nm/s (2.5 kw)	0.16*nm/s (2.5 kw)
Chuck temperature	70°C	200°C	300°C	200°C	200°C
Average film stress	-300MPa ± 75	< 300MPa	0MPa ± 20	-300MPa ± 50	-100MPa ± 50
Refractive index (@ 633nm)	1.45 - 1.50	2.07 - 2.13	2.06 - 2.10	> 1.46	2.14
Refractive index uniformity 1σ	≤ 0.50%	≤ 0.50%	≤ 0.20%	≤ 0.2%	≤ 0.2%
In-film particles (adders) >0.7µm	< 200	< 200	< 100	< 600	< 500
Mechanical particles (adders) >0.7µm	< 60	< 60	< 15	< 60	< 60

Table 1: Properties of dielectric thin films for TF-SAW applications deposited on 6" wafers with the Evatec cluster solutions, e.g. CLUSTERLINE® 200 II and CLUSTERLINE® BPM (- dynamic sputter rates).*

On the other hand, if the highest throughput is desired, nothing can beat the CLUSTERLINE® BPM deposition system equipped with a batch process module (BPM), a large turntable with multiple individual rotating chucks, and up to 5 reactive sputter sources (Figure 7b). This system can also be equipped with a wide range of in-situ process monitoring technologies for ultimate control of layer thickness and physical properties. For both deposition systems, each PVD module / station can be equipped with direct current (DC), pulsed DC or RF sputter sources, with uniformity compensation over target life. In case the deposited layers must be structured for device applications, the tools can also be configured with medium frequency RF plasma-based inductively coupled plasma (ICP) soft-etch process modules that can enable high etch rates and excellent uniformity at low bias voltages. Moreover, for depositing compound materials, the PVD module / station can be equipped with multiple sources (max. 4 RF / DC per module). Finally, to tailor the residual stress, microstructure and surface roughness of the thin films, each plasma source can be combined with an RF bias or an additional plasma generated through a magnetized capacitively coupled RF source [14].

The appeal of Evatec cluster platforms is not only that they offer best in class process solutions for the existing TF-SAW technology, but that they are also ready for the upcoming fully monolithic TF-SAW devices required by the highly integrated single-chip RF transceivers in wearables and mobile systems, for which the piezoelectric thin films (e.g. AlScN with high Sc content) are also manufactured by a PVD / PECVD process.

Typical properties of SiO_2, Ta_2O_5 and AlN layers deposited with Evatec cluster tools are shown in table 1.

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A view from Yole

RF devices & technologies focus

The mobile handset market is affected by the COVID-19 pandemic with a 9.5% decrease expected for 2020. Besides that, trade tensions between the US and China are adding uncertainties to major smartphone OEMs such as Huawei which in turn affects the whole supply chain.

Despite this, the RF front-end and connectivity industry is experiencing healthy growth. The market will reach $25 billion by 2025, up from $15 billion in 2020, with an 11% CAGR. This growth is largely sustained by the penetration of 5G in mobile handsets. Indeed, 5G adds multiple features (4x4 MIMO downlink, 2x2 MIMO uplink...) that positively impact the RF content while 4G keeps moving forward as well with more and more supported bands and use of carrier aggregation.

One important piece of the RF front-end block is the filter function. This central technology plays a major role in keeping carrier frequency bands as clean as possible and therefore helps prevent mobile handset users from experiencing slow connectivity or dropped calls.

Overall, the filter die market will increase to 76 billion units in 2025 from 56 billion units in 2019. Filters are found in a variety of formats from simple transmit or receive filters to duplexers and multiplexers as well as diplexers and antenna-plexers.

A large variety of technology platforms, either ceramic, IPD, or acoustic, is used for the manufacturing of filters in a handset. As the number of supported frequency bands in a handset is continuously increasing, along with the support of carrier aggregation and MIMO technology, there is a strong push from the industry to improve both filter size and performance.

Generally, acoustic wave filters provide better performance for out-of-band rejection and insertion loss while also offering a smaller form factor compared to ceramic and IPD based technologies. Thin film SAW (TF-SAW), as found in Murata's I.H.P. SAW or Qualcomm's ultraSAW, is particularly attractive as it fulfills size and performance requirements as well as offering an interesting cost compared to BAW technologies. Yole Développement (Yole) expects a 24% annual growth in the use of this technology until 2025.

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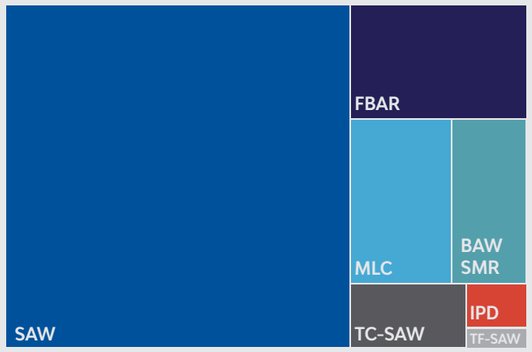
Filter volume forecast segmented by technology: LTE and 5G to drive more complex filters

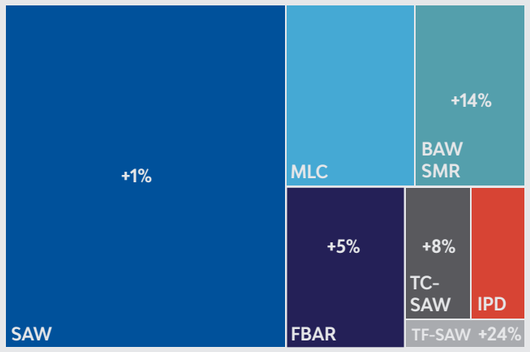
(Source: 5G's impact on RF Front-End and Connectivity for Cellphones report, Yole Développement, 2020)

- Legacy SAW filter technology will feature on organic growth
- Strong growth for high-performance filter technology (FBAR, BAW SMR, TC-SAW and TF-SAW)

56 billion filters in 2019



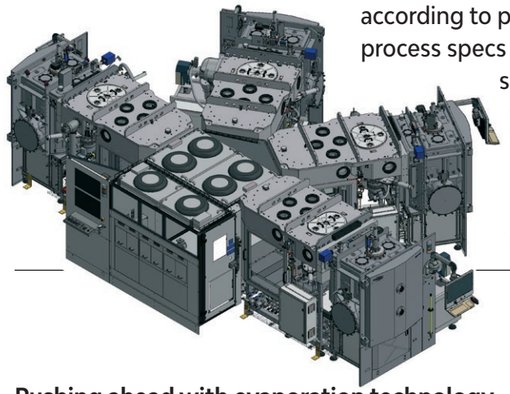
76 billion filters in 2025, CAGR +4% (2019-2025)



CLUSTERLINE® 200 delivers the ultimate in flexibility – choose from a whole range of deposition and etch process technologies across platforms configured with single or batch process modules

BAK 941 - TAKING THE "GREAT" AND MAKING IT EVEN BETTER

In LAYERS 3 at the end of 2017 we reported the drive to higher throughputs and larger 8 inch wafer sizes that had lead to a shift towards larger systems like the BAK 1401 handling 24 wafers in a single batch. Available in split chamber configuration with wire feeder technology for the e-gun sources, the so called BAK 1401 SC (split chamber) systems can deliver 10 to 20% higher throughputs according to processes. Just as importantly for the most demanding process specs however, the split chamber configuration where source chamber remains under vacuum constantly delivers improvements in process repeatability or the capability to handle sensitive coating materials which would not otherwise be possible. But now we can take the "great" and make it even better. Evatec's **Martin Kratzer** tells us how.



Pushing ahead with evaporation technology

Evaporation technology remains a hugely flexible, powerful technology for metallization and "lift off " processes in wireless communication. A huge installed base of BAK 761s, BAK 901s and BAK 1101s are in daily production around the world for the metallization and lift off processes used in production of today's SAW and BAW devices.

BAK 911 – Pushing the envelope

The BAK 911 E provides the next step in thin film production solutions for wireless applications building on the advantages of split chamber systems:

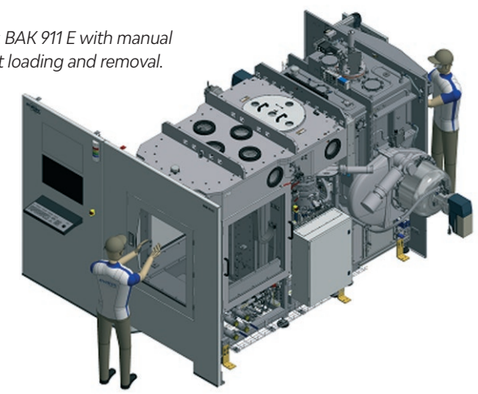
- Not just source chamber, but also the complete process chamber remains under vacuum continuously, delivering the most stable process environment possible for even greater levels of process repeatability when required.
- The only elements entering and leaving the process chamber during production are segments loaded with wafers. These enter and leave the process chamber via a load lock transfer module (LLTM). Rapid pump and transfer in this step offers a great opportunity to make additional overall gains in throughput.
- Just as in the MS Split system, sources replenished by wire feeder remain continuously under vacuum in a "ready state" for the highest stability. Opening of the process chamber itself is then limited to periodic maintenance such as shield change.
- An operator loads and unloads the uncoated and coated segments at the front-end.

Then take the next step – the BAK 941

For large volume manufacturing, integrating up to 4 tools in a cluster like the BAK 941 configuration offers even more:

- Front-end automation of wafer loading, (4, 6 or 8 inch) direct from cassette to segment and then of segment to calotte in a controlled environment eliminating risk of operator errors and reducing risk of particles / wafer damage or breakage
- Automated management and tracking of substrate journey
  - Wafer ID reading on the fly
  - Tracking of each and every wafer to an individual location / segment / process batch
  - Automated management of return of wafer to same cassette and location within the cassette after processing
- Automated handling of the required 2 inch monitor wafers for each and every calotte segment. This includes placement of monitor wafers within the segment prior to coating plus retrieval and presentation of monitor wafers after coating to separate carriers alongside each cassette.

Figure 2: BAK 911 E with manual segment loading and removal.



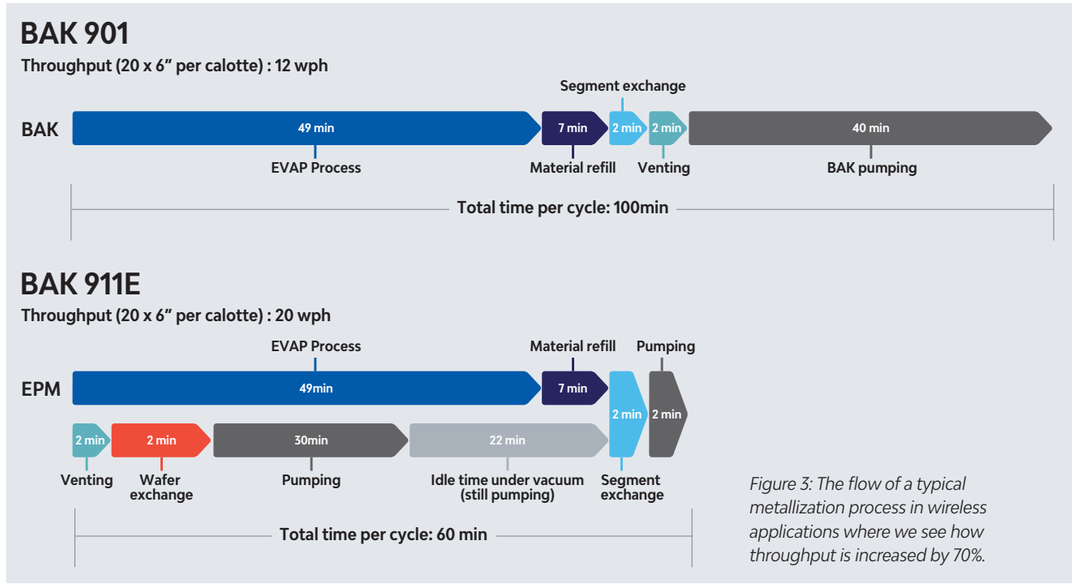


Figure 3: The flow of a typical metallization process in wireless applications where we see how throughput is increased by 70%.

Figure 4 illustrates the process flow for a BAK 941 chamber.

Enabling new thinking in fab utilization planning

Beyond the day to day advantages of enhanced throughput configuration like the BAK 941 open up other possibilities too:

Imagine being able to schedule planned maintenance for any tool within a BAK 941 cluster, automatically redirecting production to any one of the remaining tools without any interruption in work flow.

It's an exciting time for Wireless Communication

The continued impressive growth of the wireless market will continue to fuel demand for thin film production tools that increase throughput and lower cost of ownership. Emerging novel RF components enabling higher performance filters, featuring wider bandwidths and larger Q factors, will pave the way for new thin film processes too (see page 82). The thin film metallic interdigital transducer (IDT) structures required for the new so called high performance TF – SAW are just one example of where clustered configurations might just be the perfect solution.

Want to know more about the BAK 911 and 941?

If you would like to find out how these new BAK configurations could enhance your own production capabilities, why not contact your local Evatec sales and service organization.

> **Imagine increasing production output by 70% for a single tool**

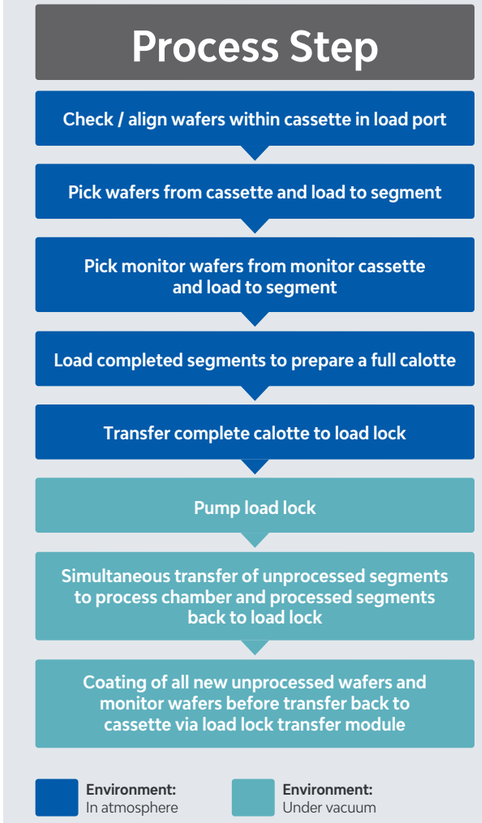


Figure 4: From cassette to coater in the BAK 941 in a few simple steps.

THANK YOU FOR READING

The 550+ strong team of engineers, scientists and support personnel based at our headquarters in Switzerland and our extensive global sales and service network are dedicated to provide products that meet and exceed your expectations.

We hope you have enjoyed reading this edition of LAYERS. We welcome your feedback about our magazine and ideas for topics that you would like to see addressed in future editions.

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Our network of local sales and service organizations around the globe are ready to support you wherever you are. You can find the locations of our country and regional hubs below. To contact the local office providing support at your specific location visit **www.evatecnet.com/about-us/sales-service**

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