LOW TEMPERATURE PVD DEPOSITION OF LOW STRESS SiN AND SiCN FILMS FOR HYBRID BONDING APPLICATIONS

Intel's ***Dr. Xavier Brun***, and Evatec's ***Dr. Patrick Carazzetti*** and ***Ewald Strolz*** investigate the feasibility of high quality low stress SiN and SiCN film deposition on Evatec's CLUSTERLINE® at low temperatures without adversly affecting tool productivity. Results confirm the possibility of achieving good uniformities (<3% 1σ) for up to 2.0µm films, and optimization of SiN film stress (100MPa) independent of film thickness.

Introduction

As transistors' density grows with each new Silicon node, the package technology needs to scale accordingly. New challenges in packaging arise as the pitch of the first-level-interconnects (FLI) shrinks below what can be achieved with solder joints. Hybrid bonding, including dielectric bonding plus direct Cu-Cu bonding, is a promising solution, but faces significant integration challenges due to the stringent requirements to enable a high yield bonding process for dielectric and Cu interfaces while maintaining low processing temperatures to ensure package integrity. Many studies have demonstrated the benefit of silicon carbonitride (SiCN) dielectric compared to silicon oxide (SiO_2) for decreasing the bonding temperature, specifically reducing the annealing temperature below or equal to 250°C. Unfortunately, these studies have leveraged plasma enhanced chemical vapor deposition (PECVD) which requires high deposition temperature (i.e., 370°C) and precursors. In addition, these films necessitate pre-bonding densification above deposition temperature to prevent voiding at the bonding interface [1-3]. PVD was recently reported to be a superior alternative method for silicon nitride (SiN) dielectric deposition for bonding applications with low deposition temperature, not requiring densification pre-bonding, and achieving comparable bond strength with low post-bonding annealing temperature [4].

Significant work on PECVD SiN and SiCN deposition of thin films on silicon substrate semiconductor device has been reported in the literature [5], of particular interest [6] reported the impact of substrate temperature for SiCN PECVD on film growth and composition. High substrate temperatures (>400°C) are needed to ensure mass transport mechanism for film deposition in addition to limiting the oxygen content in the film [6]. However, limited work has been done on the use of PVD for the dielectric film deposition process for advanced packaging applications, particularly looking at ensuring the low temperatures required for device integrity (<250°C). To this end, a set of low temperature PVD depositions of SiN and SiCN thin films on p-type (100) Silicon substrates is presented here. The deposition temperature as a function of the deposition time is characterized. In order to provide insights of handling flexibility, two hardware configurations have been tested depending on if contact on non-deposition side of the substrate is allowed. In both cases, an optimized process is presented to minimize the substrate temperature. In order to mitigate the impact of stress induced warpage at wafer level and its impact on downstream applications, the deposition process was optimized to target minimum film stress and make the stress essentially independent of the film thickness. Therefore, the film stress is characterized as a function of the film thickness. To comprehend a wide range of packaging applications, the low temperature deposition of SiN on epoxy mold compound (EMC) is also presented. The quality and hermiticity of the deposited films have been assessed on both inorganic and organic substrates with accelerated temperature and moisture bake experiments.

This study presents a comparison of SiN and SiCN thin films sputtered on a high-volume manufacturing CLUSTERLINE® PVD platform. Of particular interest is the limitation of the deposition temperature without adversely impacting tool productivity (e.g., the run-rate). The impact of the film thickness on stress and warpage is reported. Although this study focuses on blanket films, fundamentals are presented to define the best integration for packaging applications such as hybrid bond dielectric preparation for FLI bonding, or direct bond dielectric preparation to combine heterogenous materials (e.g., integrating a Si passive interposer on backside of an exposed die package for improved thermal performance).

Experimental Method

Film deposition and characterization

Magnetron sputtering is a well-established PVD technology in microelectronics manufacturing and advanced packaging for the deposition of metal and dielectric films. The main benefits of magnetron sputtering include high deposition rates, excellent thickness uniformity, tight defect control and low deposition temperatures compared to CVD and PECVD counterparts. In this work, amorphous films of silicon nitride (a-SixNy) and silicon carbonitride (a-SiCxNy) were deposited on bare silicon substrates by DC magnetron sputtering in a mixed atmosphere of nitrogen and argon. The main hardware features of the process modules, as well as the key process conditions are summarized in Table 1. A polycrystalline Si target with 400mm diameter was used to sputter SiN in a CLUSTERELINE® 300 high-volume manufacturing tool configured for 300mm wafer sizes. The deposition conditions of the SiN best-known method (BKM), such as power density, N_2/Ar gas ratio and process pressure are reported in Table 1. Two important tuning knobs have been identified to reduce the stress of SiN films. These are the use of DC power in pulsed mode, in combination with the increased process pressure obtained by pump throttling. The SiCN films were prepared on a CLUSTERLINE® 200 platform configured for 200mm wafer sizes. This tool was equipped with a 300mm diameter powder pressed SiC target, with a 1:1 silicon/carbon ratio. The process conditions of the established SiCN BKM are also reported in Table 1.

Both of the CLUSTERLINE® platforms used are both multi-chamber PVD tools with up to six process modules clustered around a central vacuum transport section. This configuration allows execution of a sequence of processes in different modules without breaking vacuum. The CLUSTERLINE® 300 configured for BSM processes, uses recessed chucks to prevent direct contact of the device side of the wafer with the pedestal surface. Only the wafer perimeter rests on a metal supporting ring located around the chuck top. The additional requirement for full face deposition in BSM applications forbids the use of any mechanical fixation of the substrate edge. Therefore, the substrate can only dissipate the heat (generated by the film growth) through radiation. To favor such heat dissipation so that the increase of temperature during deposition is limited, a simple approach was followed: alternating deposition steps with cooling steps. The implications of such "split process" on the wafer temperature and the corresponding run-rate will be discussed in Section III. Contrary to the CLUSTERLINE® 300, the CLUSTERLINE® 200 was not bound by a BSM hardware configuration. Instead, the PVD module used in this work was equipped with a clamping setup, that mechanically fixates the wafer edge by the mass of the clamping mask. As a result, the entire wafer surface is in contact with the water-cooled pedestal. Moreover, Ar gas flows beneath the substrate through a dedicated inlet at the center of the chuck and it is distributed over the entire wafer surface by a network of grooves thereby promoting efficient cooling by conduction.

In advanced packaging applications, the common practice to pre-treat a substrate prior film deposition consists of a sequence of degas and soft-etching processes [7]. Degas is applied to eliminate surface moisture from the organic films and substrates by heating the wafer typically up to 120-150°C. The subsequent soft-etching takes place in a dedicated Inductively Coupled Plasma (ICP) Etch module. Here, the bombardment of the substrate by low-energy Ar plasma effectively eliminates surface contamination and native oxides, thereby enhancing adhesion of the subsequent PVD film.

Hardware and Process Conditions	Film / PVD System	
	SiN / CLUSTERLINE® 300	SiCN / CLUSTERLINE® 200
Target	Si polycrystalline (disc Φ=400mm)	SiC powder pressed (1:1 ratio, disc Φ=300mm)
Power source	Pulsed DC (frequency=350kHz; pulse-off time=1100ns)	Continuous DC
Power density [W/cm²]	6.37	4.95
Gas ratio N_2/Ar [-]	1.0	1.2
Sputtering pressure [mbar]	$1.3e^{-2}$ (pump throttled)	$9.7e^{-4}$
Pedestal type	Clampless, recessed chuck top, PCW cooled pedestal	Clamped, flat chuck top with back-gas inlet, PCW cooled pedestal
Pre-treatment process	Radiation degas (load-lock) and ICP-Etch	ICP-Etch

Table 1: Hardware configuration and process conditions used to sputter deposit SiN and SiCN films.

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Low temperature SiN reliability assessment

In this section, the focus is on reliability of the low temperature deposited films. SiN films were deposited on both inorganic materials, i.e. p-type (100) Silicon substrate, and organic materials, such as EMC on a Si substrate, to comprehend a wide range of packaging applications. All the samples were processed using the same low temperature process described above on the 300mm tool. To improve the adhesion to the organic material interface, this study includes understanding the impact of an ICP-etch step pre-deposition. To envelope a range of mold materials available, two different mold compounds were compared side by side. As shown in Table 2, liquid and granular EMC have different mechanical properties particularly Young's Modulus and Coefficient of Thermal Expansion (CTE).

	Sample		Mechanical Properties	
	Stack	Interface Material	CTE [ppm]	E [GPa]
Inorganic	1.5µm SiN 775µm Si	Silicon	2.3	170
Organic	1.5µm SiN 100µm Mold 775µm Si	Granular EMC Liquid EMC	5.0 16.0	20 9

Table 2: Material properties - SiN reliability experiments

After deposition, standard diamond dicing was used to singulate the wafers into samples that were then submitted to Temperature/Humidity plus preconditioning (JEDEC standard J-STD-020 [8]) and extreme preconditioning for margin assessment and HTSL/Bake (JESD22-A103 [9]) to accelerate SiN de-lamination and dielectric cracking failure modes. The cracking in SiN results from moisture assisted crack growth propagation. Macroscopic and microscopic inspections were performed to detect the presence of defects such as SiN cracking, flaking, fringing, etc., both post singulation and post temperature/humidity exposure.

Results and discussion

Films performance summary

In this experimental study, various SiN and SiCN films with thickness ranging from 100nm up to 2.0µm were sputtered on bare silicon wafers and were characterized without performing any densification or annealing. Spectroscopic ellipsometry (Woollam M-2000) was used to measure film thickness, refractive index (n) and extinction coefficient (k). In-wafer statistical data was collected using a 49-points circular pattern with 6.0mm edge exclusion. The film uniformity is an important metric to characterize the quality of a deposition process. The uniformity criteria adopted here is "1σ", which is defined as standard deviation of the thickness distribution divided by the average. The film density is calculated based on the mass difference of the wafer pre- versus post-deposition. Table 3 summarizes data measured on 2.0µm-thick films of SiN and SiCN. The obtained 1σ uniformities are below 3% for both films. These values can be considered satisfactory and show that the PVD processes developed are suitable for depositing high-quality films at least up to 2.0µm with deposition rates in excess of 20.0Å/sec. We measured a SiN refractive index of 2.11. This can be compared to published n values ranging from 3.18 to 2.1 with N/Si ratio increasing from 0.31 to 1.5 [10]. The measured density of the 2.0µm SiN film is 2.7 ±0.05 g/cm^3. This value matches well with published data of 2.8 g/cm^3 for a film with N/Si ratio of 1.1 [11] and 2.28 to 2.97 g/cm^3 depending on the deposition pressure [12]. The refractive index of the SiCN film is 2.29 and the corresponding density is 3.5 ±0.5 g/cm^3. Published data show a direct relationship between increase in the nitrogen content in the film and the concomitant increase of both density and refractive index. Inoue et al. [3] reported a refractive index of 1.95 and a corresponding density of 1.98 g/cm^3.

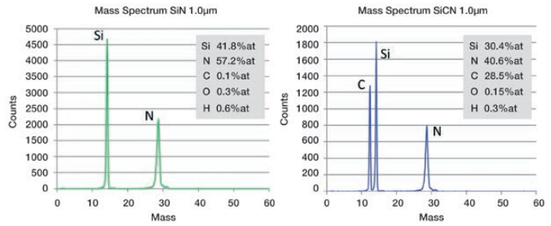
Performance	Film / Substrate	
	SiN / 300mm wafer	SiN / 200mm wafer
Deposition rate [Å/sec]	20.71	23.68
Thickness uniformity, 1σ [%]	2.97	1.62
Refractive index, n @633nm [-]	2.11 (3.18-2.1 in [10])	2.29 (1.95 in [3], and 2.1-2.3 in [13])
Density as-sputtered [g/cm^3]	2.7 ± 0.05 (2.8 in [11,12])	3.5 ± 0.5 (1.98 in [3])

Table 3: Properties of 2.0µm SiN and SiCN films

Elastic recoil detection analysis (ERDA)

ERD analysis uses high-energy heavy ion beam to determine the elemental depth concentration profiles in thin films [14]. In this work, the analysis was performed on selected samples of 1.0µm SiN and 1.0µm SiCN by 13 MeV 127I Heavy Ion ERDA. The elemental composition was retrieved from the bulk of the film at a depth of about ~30-150nm so that the surface contamination is not considered. ERD spectra of SiN and SiCN films are displayed in Figure 1. The empirical stoichiometry formulas reported in Table 4 were established based on the elemental composition normalized to Si. In the case of SiN, a normalization factor of 3 was used; whereas, in the case of SiCN the normalization factor was 1.

The ratio of Si to N in the silicon nitride film is 3 to 4.1, indicating that a nearly stoichiometric Si3N4 is formed. The other elements in the measured mass spectrum: C(<0.1%at), H(<0.6%at) and O(<0.3%at) are present as impurities. Published research shows that the N/Si ratio can be tuned between 0.56 (under-stoichiometric) and 1.33 (stoichiometric) depending on the N2/Ar ratio in the process atmosphere [15]. The ratio of Si to C in the SiCN film is 1 to 0.99, which validates the nominal composition of the target. Beside the target elements and nitrogen, experimental data show a very minor content of H (<0.3%at) and O (<0.15%at). In the linear scale spectrum such low content of H and O is not visible. The composition of SiCN produced in this work is richer in nitrogen and it is substantially hydrogen-free compared to the published data [3].



Film	Empirical formula				
	Si	C	N	H	O
SiN	3	0.006	4.1	0.024	0.041
SiCN	1	0.99	1.40	0.01	0.005
SiCN [3]	1	0.79	0.75	0.62	0.003

Table 4: Empirical stoichiometry formula of sputter deposited SiN and SiCN films derived from ERD analysis

Wafer temperature and stress vs. film thickness

The maximum temperature of the wafer during deposition was measured using thermal labels (Celsistrip® Spirig – Switzerland). These labels use a scale of markers reacting at a progressively higher temperature in steps of 5-6°C, which represents the measurement resolution. Each marker turns to black when triggered, thereby indicating the peak temperature reached during process. In our tests, the thermal label was placed on the deposition side at the center of each monitor wafer. Figure 2 compares the process temperature versus the film thickness for SiN films produced on CLUSTERLINE® 300 (split deposition process), and SiCN films produced on CLUSTERLINE® 200 (single step deposition process).

The strategy of splitting the deposition process alternates deposition steps of 100nm (equivalent to a process time of 47.0sec) followed by a cooling step of 60sec. Five different films with thickness ranging from 100nm up to 2.0µm were deposited in this process regime. Prior to PVD, each monitor wafer was pre-treated with degas and ICP-etch, which resulted in a peak temperature of ~150°C. The peak temperature post PVD shows an increase to ~180°C for the 100nm SiN film, up to ~207°C for the 500nm film and then a stabilization to ~228°C for all other thicker films (♦ markers in Figure 2). This behavior indicates the effectiveness of the deposition/cooling regime adopted to stabilize the peak temperature. As a comparison, SiN deposition of 300nm, 500nm run in a single step without cooling reach ~40-50°C higher temperature (▲ markers in Figure 2), and the 1.0µm process exceeded the upper range of 260°C.

SiCN processes run on CLUSTERLINE® 200 indicate a stable temperature of ~100°C, independently from the film thickness (● markers in Figure 2). In fact, it was shown that 100°C substrate temperature was reached already during the ICP-etch prior deposition. This highlights the effectiveness of the hardware setup combining mechanical wafer clamping and active back-gas cooling.

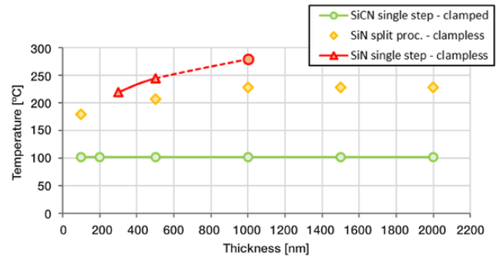


Figure 2: Peak wafer temperature corresponding to SiN and SiCN films of various thickness processed either in single deposition step, or split process, respectively.

An additional set of wafers processed with the same condition was used to characterize the residual film stress. The in-plane stress was measured by recording the change of the curvature radius of the substrate induced by the deposition process [16]. The wafer curvature and bow were measured optically with a stress analyzer Tencor FLX-3300-T. The well-known Stoney's formula was used to relate the measured substrate curvature to the residual film stress, σ as:

$$\sigma = \frac{E_s}{6(1-\vartheta_s)} \cdot \frac{t_s^2}{t_f}\left[\frac{1}{R_1} - \frac{1}{R_0}\right]$$

Where Es/(1-v_s) is the biaxial Young's modulus of the substrate (180.5 GPa for (100) oriented Si wafers), ts and tf represent the thickness of substrate and film, respectively. R0 and R1 are the curvature radii before and after deposition. The measured stress as a function of the

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film thickness are displayed in Figure 3. Both SiN and SiCN films exhibit a compressive stress level, which becomes more moderate as the thickness increases. Particularly, a stabilization is observed when the film thicknesses exceeds 1.0µm. In the case of SiN, a plateau is reached at -65 ±5MPa, whereas the stress of SiCN films levels off around -280 ±20MPa. Residual compressive stress level means that the deposition process has produced a dense and compressed film, which tends to expand in order to relax its internal energy. In this case, the film expansion exerted on the substrate results in a convex warpage [17]. In the worst-case scenario, a highly compressive stress distribution can lead to catastrophic failure mechanisms, such as film buckling, blistering or peeling off. However, the moderate compressive stress of SiN films obtained in this work should not represent concerns of the film integrity, or subsequent integration and device reliability issues. The minimization of SiCN stress can also be investigated by using tuning knobs, such as DC sputtering in pulsed mode and pressure modulation, similarly to SiN. This will be addressed in future work.

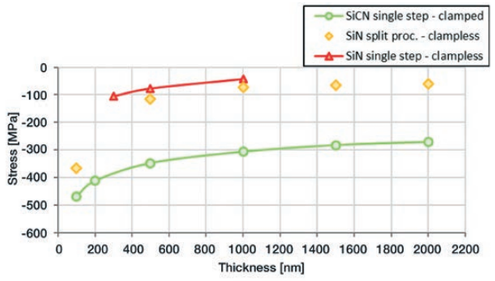

Figure 3: Film stress a function of the thickness for single step SiCN deposition process, and single step versus split process

Run-rate vs. film thickness

In order to keep a viable tool productivity, especially when processing thick films with stringent temperature requirements, it may be necessary to have more than one deposition chambers. This section provides some guidelines to establish the suitable tool configuration based on the required film thickness and the run-rate goal. The run-rate defines the tool output in terms of number of wafers per hour processed from job start to end. Different scenarios have been considered and executed on the HVM platform equipped with one ICP-Etch and up to four PVD chambers. The run-rate figures are reported in Figure 4.a (split deposition process like SiN) and Figure 4.b (single-step deposition).

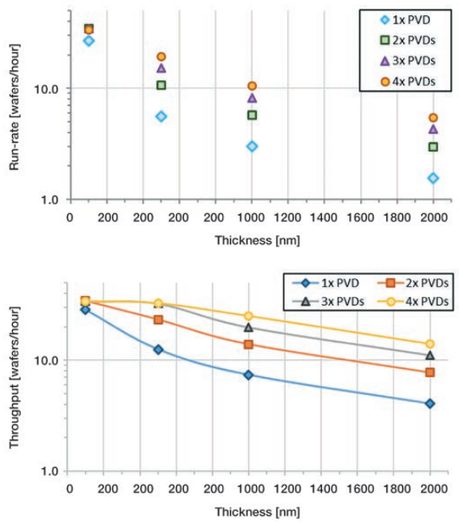

Figure 4: Run-rate vs. film thickness and number of PVD chambers: (a) SiN split deposition process with cooling steps, and (b) SiCN single step deposition process

Stress Test Results

Stress test experiments were performed with low temperature SiN layer singulated samples on two types of EMC and the Bare Si. For the EMC samples, ICP etch was studied to understand its impact on the SiN to EMC adhesion. For each leg, a total of 6 units were used. Table 5 summarizes the reliability results for all the samples. For the silicon samples, no gross delamination was observed on all the conditions. This is because the CTE mismatch between Si and SiN is lower, which leads to lower shear stress at the interface as the temperature changes. Thus, the risk for the interfacial delamination is lower than the one for the organic samples.

Type	Sample		Reliability results [# units with delamination/total units]		
	Mold type	Pre-Etch	168hrs 60°C / 60% RH +10x reflow 260°C	216hrs 30°C / 60% RH + 3x reflow 260°C	1000hrs 150°C
Inorganic	None	No	0/6	0/6	0/6
Organic	Granular	No	6/6	6/6	0/6
	Granular	Yes	0/6	0/6	0/6
	Liquid	No	0/6	2/6	0/6
	Liquid	Yes	0/6	0/6	0/6

Table 5: Low temperature SiN reliability results

All the units were also inspected for SiN cracking optically. Only the units with no etch showed SiN cracking for both granular mold and liquid mold, with the latter being less severe (Figure 5). Although Liquid mold having higher CTE mismatch shows better performance than granular, this could be due to its much lower young's modulus and more significant stress relaxation for liquid mold material [18]. Blade dicing impact on SiN was also analyzed side by side for all the samples at time 0 and post reliability test. Si substrate and all organic non-etched samples showed fringes representing SiN delamination at the edge of the sample in Figure 6. Note that no delamination extension was observed post reliability on the Si substrates. A clear benefit was observed with the addition of the etch process for both organic materials. In addition, it was observed that granular mold singulation chipping performance was qualitatively better than the liquid mold material, which could be explained due to its higher hardness or young's modulus.

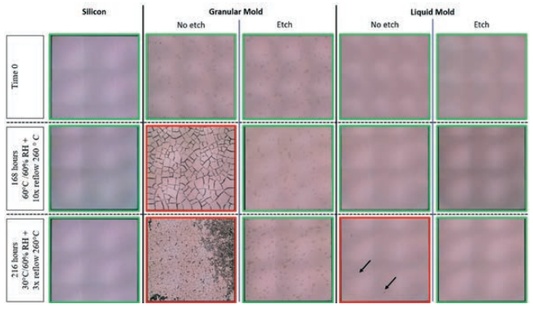

Figure 5: Low temperature SiN surface macro inspection (3x diopter) on organic and inorganic substrates with and without etch at time 0 and post reliability testing

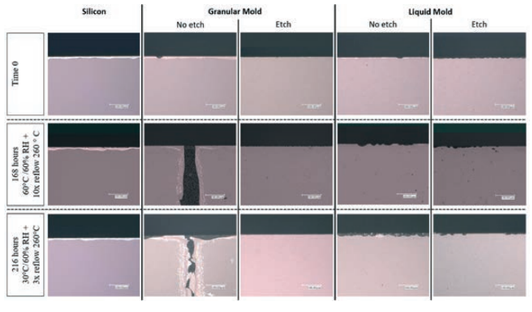

Figure 6: Low temperature SiN surface and singulated edge micro inspection (20x microscope) on organic and inorganic substrates with and without etch at time 0 and post

To further investigate the low temperature SiN delamination mechanism, additional inspection was carried for the granular EMC post reliability. Massive cracks in nitride are observed throughout the sample at 20x (Figure 7a). By looking at higher magnification, areas of flaked nitride were observed along with exposed mold (Figure 7b). Exposed mold showed areas of small filler pull out with intact large fillers (Figure 7c). Bottom of flaked nitride was inspected (Figure 7d) and revealed presence of small fillers indicating cohesive failure within the mold. Energy dispersive spectroscopy (EDS) confirmed the presence of mold fillers at the bottom of flaked nitride (Figure 7e).

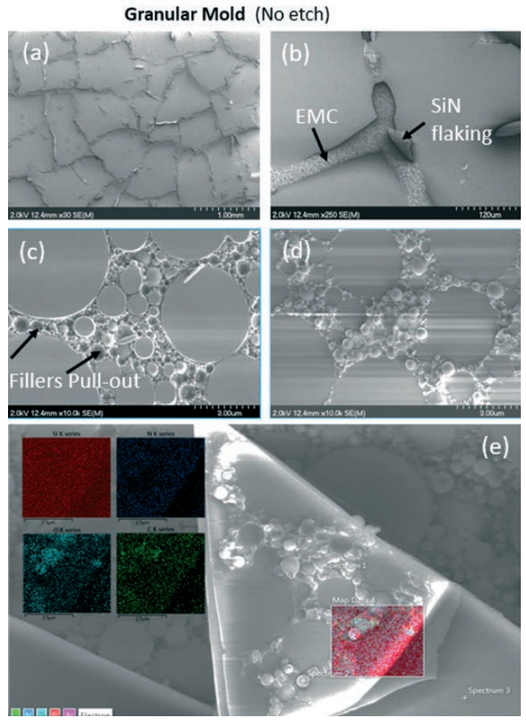

Figure 7: Low temperature SiN surface inspection (SEM) on granular EMC substrate without etch post reliability. a) Gross SiN cracking observed at 20x, b) Mold exposed and SiN flaking observed at 250x, c) Exposed Mold area without SiN (delaminated area) at 10kx, d) Bottom of SiN (delaminated area) at 10kx, e) EDS analysis on bottom of SiN confirming mold filler pull out

Although, within mold cohesive failure was observed for granular mold, it is still important to understand the influence of etching. As mentioned earlier, soft etching is generally performed to clean surfaces before deposition. This would not explain the difference in performances between the liquid and granular mold observed in the reliability tests. Therefore, additional characterization with atomic force was performed demonstrating the etch impact on surface roughness. In all cases, etch increased the roughness of the mold compound, therefore, increased the contact area with the deposited nitride. As a result, it provided better mechanical interlocking of the SiN film with the organic material (Figure 8). Interestingly, unetched liquid sample showed higher roughness compared to granular mold that may explain the reliability difference.

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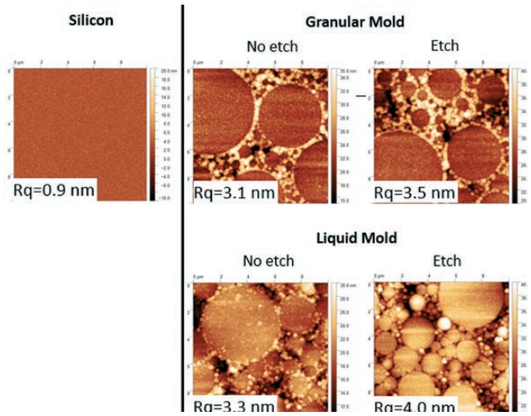

Figure 8: Low temperature SiN surface roughness measurement (AFM) on organic and inorganic substrates with and without etch at time 0.

Conclusion

A low temperature PVD dielectric deposition process has been demonstrated both for SiN and SiCN thin films. This helps Hybrid bonding integration and ensure package integrity by lowering the deposition process temperature. PVD of SiN and SiCN films with good uniformity for up to 2.0µm film thickness was demonstrated. Residual stress was characterized to understand its impact on the wafer warpage. For both dielectrics, above a minimum film thickness, the stress becomes almost independent of the film thickness. The SiN process was optimized to near zero stress (~50MPa compressive) on Silicon substrate, indicating a minimized impact on wafer warpage. The criticality of the substrate cooling was observed. Two different deposition approaches were presented: one by splitting the process with deposition and cooling cycles; the other by leveraging an improved cooling path for the substrate. Both approaches showed effective substrate temperature control, with the later had less impact on the run-rate. Compared to PECVD films, which use precursor gases, PVD films are free of impurities and do not require any densification (annealing). Industry usually requires above deposition temperature densification to prevent voiding at the bond interface. The PVD deposited SiN composition showed low Hydrogen content. The SiCN PVD obtained was Nitrogen rich compared to PECVD films, its chemical composition on Bonding performance will be investigated in the future.

Reliability of SiN was studied on both inorganic and organic interfaces. Films' quality and hermiticity were assessed with accelerated temperature and moisture bake experiments. Adding ICP-etch on EMC before SiN deposition improved film adhesion with an increased surface roughness and samples survived all the stress conditions, while un-etched samples exhibited SiN cracking and delamination.

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Updates

Results for SiCN films sputtered on 300mm are also now available