CLUSTERLINE® 600 Perfect for next generation IC-substrates too!

The potential benefits of moving from wafer to panel processing including much higher material and process utilization are already well documented (Figure 1). Evatec's Senior Product Marketing Manager ***Roland Rettenmeier*** takes us through some of the recent developments on the well established CLUSTERLINE® 600 platform. These updates in capability make it the perfect choice for customers when setting up manufacturing capability for emerging markets like advanced IC-substrates for applications such as Artificial Intelligence, and other High Performance Computing applications.

innovation
onto

Evatec Collaborates with Onto Innovation in Panel Level Packaging Applications Center of Excellence

To find out more about the co-operation read the article

Advanced Packaging Technologies for the future – Building on a common portfolio of process technologies

Evatec's CLUSTERLINE® 300, CLUSTERLINE® 600 and HEXAGON, feature the same process concept for Advanced Packaging:

- Atmospheric batch degas for preparing substrates with organic load for best in class vacuum processing
- ICP or CCP Etch technology (with arctic cooling) for highly uniform etch prior to deposition
- Long life PVD sources for lowest cost of ownership in high volume manufacturing

CLUSTERLINE® 600 – A proven pedigree in high volume manufacturing

Evatec's CLUSTERLINE® 600 panel processing tool was built leveraging the know-how gained across Evatec's wafer level processing platforms over many years and has already established itself as the market leading system for panel processing. Built around a central Vacuum Transfer Module (VTM), the tool can be equipped with up to 5 single process modules (SPM) for etch or deposition. An atmospheric front end module (AFEM) handles substrates in and out of FOUPS stationed on up to 6 Load Ports (LP). Pre-processing via Evatec's unique Atmospheric Batch Degasser (ABD) followed by two stage pumping brings substrates into vacuum in perfect condition for any etch and deposition processes. A typical configuration is shown in Figure 2.

By the start of 2024 there were more than 10 CLUSTERLINE® 600 working in volume manufacturing around the world. The latest developments on the tool make it ready to handle next generation IC-substrates.

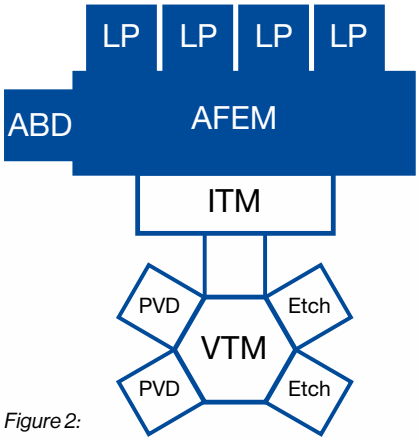


Figure 2:

Panel Level Packaging – Bringing much higher material and process utilization

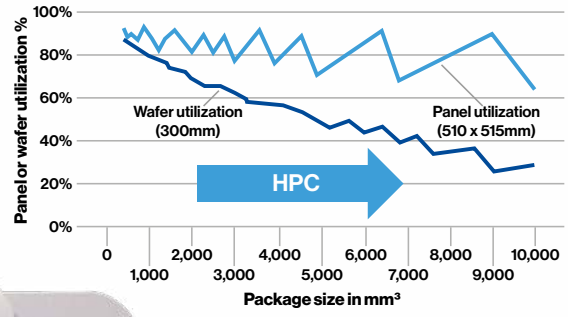
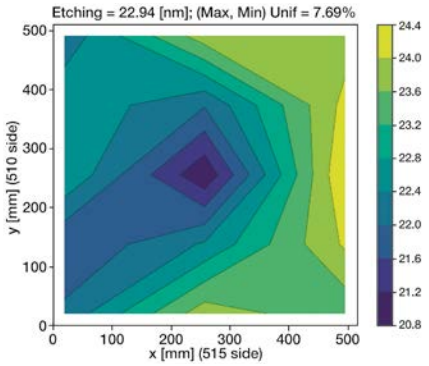


Figure 1:

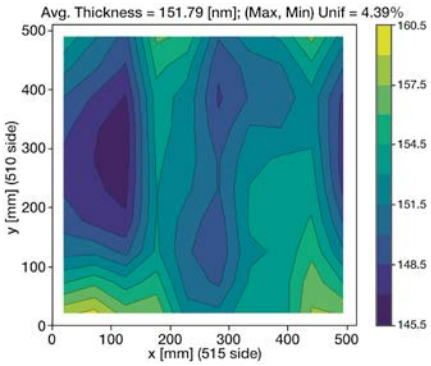
Some typical process results

Low contact resistance (R_c), excellent adhesion and low particles are paramount. Typical process performance results of etch and deposition processes for Ti and Cu are shown below.



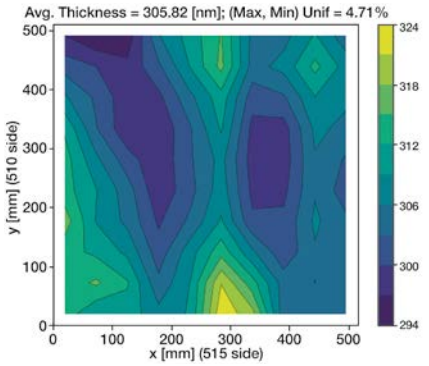
Etch

Etching uniformity better than 10%, for etching amount of 20nm (SiO_2 equivalent), with etch rate higher than 0.15nm/s.



Ti deposition

Thickness uniformity better than 6% for 150nm Ti deposition. Sputter rate higher than 100nm/min and Rs ≤ 75 uOhms*cm.



Cu deposition

Thickness uniformity better than 6% for 300nm Cu deposition. Sputter rate higher than 200nm/min and Rs ≤ 3.5 uOhms*cm.

New tool features now available

Ready for advanced substrates

Newly designed end effectors for handling thin substrates down to 100µm thickness and recessed chucks with full "Keep Out Zone" (KOZ) functionality ensure that active areas are not touched during handling and processing.

High performance robust handling – flipping

The latest AFEM design can accomodate up to 6 Load Ports and features a substrate flipper for double sided processing.

A view from Yole Group

The Glass era starts in the advanced IC substrate and semiconductor equipment industries.

The advanced packaging industry is at a new inflection point with the arrival of glass as a new core material. Announced by Intel in September 2023, this next generation of Advanced IC substrates will be adopted to overcome the limitations of organic core substrates and easily meet the demands of high-performance computing (HPC) and AI trends, opening new options such as flexible form factors and better mechanical stability.

Glass, as a material, offers superior dimensional stability, thermal conductivity, and electrical properties compared to the built-up organic substrates. However, glass introduces challenges in handling and processing, requiring precise care during manufacturing. Additionally, inspection and metrology processes for glass substrates necessitate specialized equipment to ensure quality and reliability.

Despite these challenges, the adoption of glass core substrates is driven by the demand for larger substrates and the technological trend toward chiplets and heterogeneous integration.

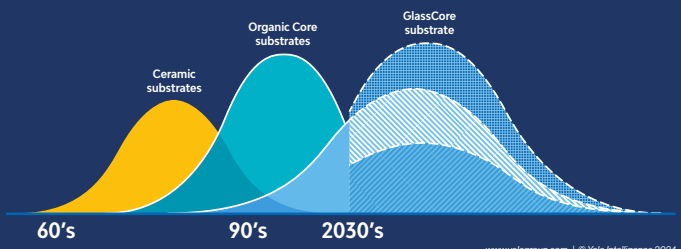
Within this landscape, Through Glass Via (TGV) technology is crucial, facilitating higher connection density and superior signal integrity for high-speed circuits. While TGVs offer performance benefits, they also present manufacturing challenges and higher production costs. Recent advancements in TGV-related patents are aiding the commercialization of glass core substrates.

The synergy between glass core substrates, organic core substrates, and panel-level packaging (PLP) is driving the adoption of panel-adapted equipment by offering enhanced chip density, reducing costs, and improving manufacturing efficiency and yield. As GCS technology matures, it promises to redefine the advanced packaging landscape, particularly for AI accelerators and servers, paving the way for next-generation chip designs and packages.

The increasing growth of AI and its next-generation AI accelerators is driving a significant increase in chip package sizes. Current AI accelerators typically have package sizes around 70 to 80 mm. However, the growing need for larger packages, exceeding the limits of organic substrates at 120 by 120 mm, presents a challenge to the advanced packaging industry. To address this demand and offer a cost-effective solution, the industry is shifting towards panel utilization and related equipment, enabling the production of larger chip packages at reduced costs.

Market adoption trends of Glass Core Substrates

Source: Satus of the Advanced IC Substrate Industry report, Yole Intelligence , 2023



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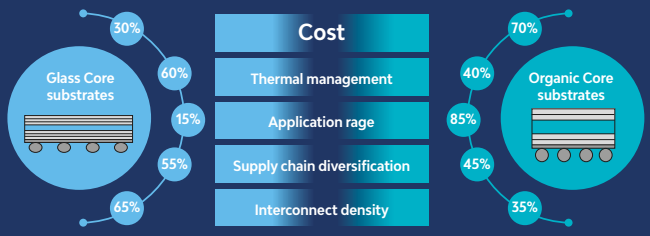
Advanced IC Substrate – comparison with Organic Substrate material

Source: Satus of the Advanced IC Substrate Industry report, Yole Intelligence , 2023



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About the author

Bilal Hachemi, Ph.D., is a Technology & Market Analyst, Semiconductor Packaging at Yole Group.

Working within the Manufacturing & Global Supply Chain activities at Yole Group, Bilal contributes daily to the analysis of packaging technologies, their related materials, and manufacturing processes.

Previously, Bilal carried out experimental research in the field of nanoelectronics and nanotechnologies, focusing on emerging dielectric materials and their ferroelectric applications. He (co-) authored several papers in high-impact scientific journals and participated in several international conferences.

Bilal obtained a Ph.D. in nanoelectronics in 2022 from the Grenoble Alpes University (France), and he studied at IAE Grenoble for a management master's degree.