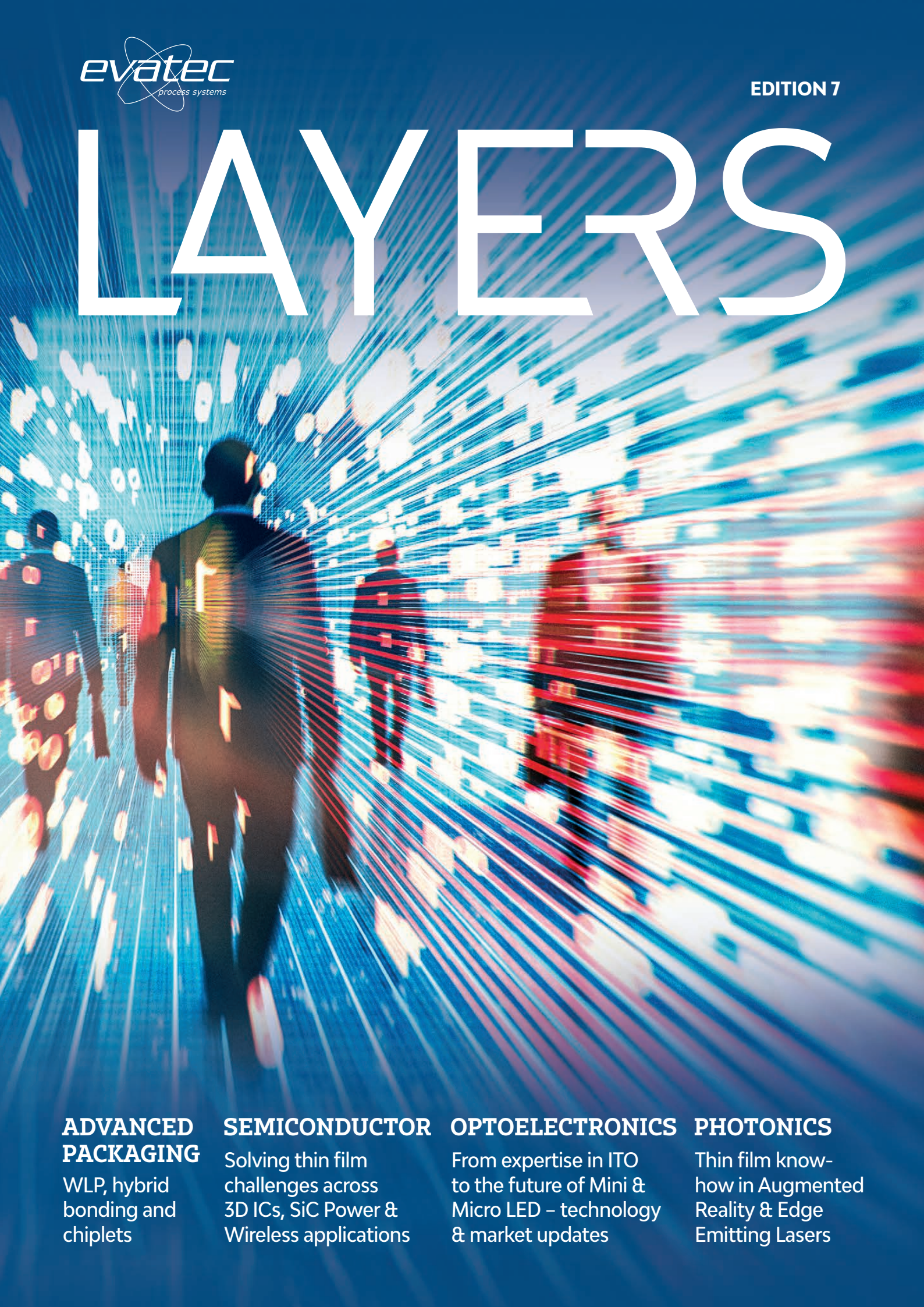
evatec
process systems

EDITION 7

# LAYERS



**ADVANCED PACKAGING**
WLP, hybrid bonding and chiplets

**SEMICONDUCTOR**
Solving thin film challenges across 3D ICs, SiC Power & Wireless applications

**OPTOELECTRONICS**
From expertise in ITO to the future of Mini & Micro LED – technology & market updates

**PHOTONICS**
Thin film know-how in Augmented Reality & Edge Emitting Lasers

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**Photography**: Peter Fuchs / www.fuchs-peter.ch

> Evatec technology has been shaping the world for 70 years

# "SETTING SAIL" FOR AN EXCITING FUTURE

**It has continued to be an exciting time for our sector since the publication of our last LAYERS 6, with the strong investment seen in 2021 continuing through 2022. Indeed, fab equipment spending reached close to USD 110 Billion by year end 2022[1]. This was at a time when global supply chains had already been under pressure as a result of the COVID pandemic, and even had to ramp up to meet the new levels of demand.**

As a company we have already taken a number of measures to grow both our manufacturing capacity and flexibility for the future including enlarged assembly areas. Maintaining strong long-term partnerships and working closely with both suppliers and customers is more important than ever as we look to enjoy the benefits of strong long-term industry growth all together.

While customers have been expanding their production capacity, they have also been setting us new challenges in process performance. As a result, 2022 was also an important year for product innovation at Evatec. Highlights included the launch of the new HEXAGON offering both lower $R_c$s and higher throughputs in packaging applications and Evatec's ground breaking BAK 911 and MULTI BAK clustered evaporation solutions delivering new levels of process repeatability and lowering cost of ownership for high volume wireless applications.

I hope you will find something to inspire you in 2023 in this, our seventh addition of LAYERS. As always, we welcome your feedback about our products and services and look forward to meeting you during the year.

**Andreas Waelti CEO**

*[1] Numbers according to SEMI.org*

# CORPORATE NEWS



> The company, market and technology news stories reported in this year's Corporate and Business unit chapters would not be possible without our people. They are at the heart of everything we do. My sincere thanks go out to everyone involved for their support in the production of LAYERS 7.

**Allan Jaunzens**
Head of Marketing and Communication

# EVATEC EUROPE: AT THE HEART OF EVATEC'S GLOBAL ORGANIZATION

**Evatec's European sales and service organization has also seen huge changes over the last 20 years. European Managing Director *Ralf Eichert* talks about how things began and where his organization is today**

> "I see huge enthusiasm amongst industry colleagues in Europe with a positive 'can do attitude'"

### You and your team have been taking care of business for Evatec since its foundation in 2004. What have been the biggest changes in that time?

Of course the transition at the start from the well established brand of Unaxis to a small unknown company was a huge change both for employees and customers. However, the initial motives of investing in and driving BAK technology forward under its own brand were well understood by customers and we were able to quickly show them positive results as a small agile company that could be flexible in its approach. Another significant milestone was the acquisition of the systems business from Oerlikon in 2014 and integration of Evatec and Oerlikon cultures to build up an exciting new future orientated team.

### How has the nature of the business changed over the last 18 years?

As a brand, we changed from an evaporation equipment supplier focused on relatively small niches within semiconductor to a true global supplier for thin film solutions across wider markets including Packaging, Optoelectronics and Photonics. Within Europe in particular we have developed strong technology development partnerships with both academic and industrial research groups. We have invested heavily in building up the R&D facilities and process know-how to support customers at our European headquarters in Truebbach. Major European players have then gone on to roll out processes and technologies developed together with us to their manufacturing sites in Asia.

### How has your local team and the way you work changed over that time?

Of course we have grown significantly in size. Back in 2004 our sales and service organization started with around 10 people across the whole of Europe and today we are around 60 but we have also grown in breadth of knowledge too. Customer expectations for the level and speed of service available from us have also changed over the last 20 years. Stronger technical support within customer service coupled with additional new functions in our team like technical market management and application support have helped us become stronger local partners.

As our partnership with global customers has grown we have introduced key account management to improve information flow, maintain quality and consistency in how we support them. We have strengthened internal business processes to manage the increasing complexity of our products while new software platforms have improved collaboration between ourselves, suppliers and customers making data available to everyone 24/7 at the touch of a button.

### What do you see as Europe's strengths in our industry and how do you see things developing in Europe in future?

I see huge enthusiasm amongst industry colleagues in Europe with a positive "can do attitude". They are keen to develop and use their technical know-how to innovate. Our Multicultural teams are broader than ever and are well placed to help Europe lead the world in exploiting communications, healthcare and computing opportunities offered by new areas such as Quantum technology, while broader Government initiatives (e.g. US Chip Act) will offer opportunities to drive advances in manufacturing that increase capacity and lower costs.

However, I see challenges too, not just the uncertainty brought by the difficult political situation within Europe and elsewhere right now but also be the limited human resources available to our industry at a time when we want to grow. Attracting and retaining young talented people when they have so many opportunities available to them is an ongoing task where we must all invest as an industry over the coming years.

### How do you see your local European organization developing in future?

In general I see the existing trend to expand knowledge and offer more and more customer value from our local organization continuing. As our long term cooperation with customers gets even closer and we grow and extend our markets supporting more new products and applications we will certainly need people with new technical skills too. The ongoing drive to digital transformation with access to better "data" that can be analysed more easily is also critical, whether it's in the initial design process of our products or the monitoring of their real time performance in the field. Easier access and sharing of better data will help us make better informed decisions more and more quickly. Helping our European sales and service organization be ready for the future is one of my key tasks and it's one that I love. ◻

# Becoming the number

# ONE

## Vision

Enriching people's lives by enabling innovations in connectivity & mobility, data processing, energy efficiency and smart sensing.

Our company has grown hugely since 2004 when we delivered our first BAK tools. In 2022 we were proud to deliver our 1000th tool under the Evatec brand. So here are some statistics about our company and our people today ...all sharing in one goal to help our company become the partner of choice in thin film technology.

> "More than 40,000 substrates processed per year in our ECL"

## Our Business

**4**

**Business Units**

**17 market segments in total across Advanced Packaging, Semiconductor, Optoelectronics and Photonics**

## Our Progress

**270M**

**Sales of CHF 270M in 2022**

**8 core production platforms, more than 1000 tools delivered / installed worldwide since 2004**

## Our Technology

**>500**

**Patents**

**4 core process technologies – Evaporation, Sputter, Etch and PECVD**

## Our Manufacturing

**>40**

**Systems assembled simultaneously**

**Manufacturing capacity for customer orders in three assembly halls**

## Our People

**>600**

**employees globally**

**>35 nationalities**
**>15 office locations**

## Our R&D

**3000 m²**

**application laboratory**

**Down to ISO 4 with 30 tools, 40 measurement techniques**

# WHY WAIT? GET THE MOST OUT OF YOUR EVATEC TOOL

**Evatec's Retrofit Manager *Mehmed Ljatifi* talks about the different benefits retrofits can bring for existing tools, how the retrofit department operates and explains why good preparation is key to success**

### Tell us how you help your customers?

As a Service Department, we want to show our customers the untapped potential of their systems and how they can access that through retrofits. That could be anything from tackling obsolescence to improve uptime, to adding new hardware / process capabilities or even individual customized solutions. As Evatec's Retrofit Manager, it's my job to organize and streamline the business making sure things run smoothly for the customer. We do this with a team of system specific project managers who collaborate closely with our Product Lines Department as well as the individual business units. The focus is on our customer and their needs to make sure they get the best payback for their investment.

### Why are project managers necessary in your team?

Just like customers, every retrofit is at least slightly different even if it looks the same at first glance. We need to work with system specific project managers with a good understanding of the platform and how it has changed over the years. Retrofits can of course also be very complex. An understanding for the whole system and its configuration options needs to be mastered including the specific customer tool and its history. We need to be sure that retrofits we make to address one aspect of performance don't adversely affect another. Only then is it possible to make sure all new elements can be integrated successfully.

### What is the difference between machine upgrades and a classic parts replacement? Where is the added value for the customer?

Of course we deal with consumables and other spare parts which can be just replaced 1:1 without further effect on the tool. Classic parts replacement is a "plug and play" story whereas a retrofit is normally much more complex. We define retrofits as where there is a change to the "bill of materials". Retrofits often need software upgrades too. Depending on the complexity of the retrofit it could often involve a much more expensive initial capital outlay, but if we talk about losing USD 1'000.- every hour caused by tooldown, it is self-evident, that every retrofit that brings improvements to tool uptime can easily bring added value for the customer.

Depending on the type of retrofits we can bring a tool back to "new" to extend its working life, expand its capabilities to run processes it couldn't before, or increase its throughput.

Bringing a customer's system fully up to date also brings other benefits too, including reducing unexpected problems. Evatec's comprehensive knowledge through its "digital twin" can also enable improved technical support at all levels.

>>>>>

*Below is a simple guide to the differences between spare parts and a complete retrofit*

**Spare Part**

**Definition:** A spare part is an extra piece, replaceable component (1:1), or identical to and interchangeable with the item.

- Quote provided by local organization
- In most cases the customer can replace the themselves

VS

**Retrofit**

**Definition:** Means a change or modification or improvement made to an equipment / assest that improves the performance, capacity and or capability of such asset.

- Definition of customer hardware / process specification
- Quote provided by Customer Service
- Installation done by Evatec

## Types of retrofits

### Tell us more about the different types of retrofits?

There are 3 different reasons why a customer should think about retrofits:

### Obsolete Parts

**Reason 1**

Tackling obsolescence is one of the most common reasons. For tools which have been in service for many years, the risk of long tool downs caused by important but obsolete parts breaking gets bigger. The reasons for retrofits could be the same for 2 tools but the retrofit could still differ. Let's explain it with the example of a power supply upgrade on a BAK tool. Upgrading an old EHV to the current standard EHV 510 for a customer in the US is not the same as for a customer in Europe, because an additional transformer needs to be bought by the US customer as they first need to step down from 460V to 400V. However, customers often gain additional benefits in other areas even when they retrofit for obsolecsence too. Take an obsolete server that needs to be upgraded as an example. New software will be available with many additional functions and therefore enhanced capabilities.

### Enhanced Capabilities

**Reason 2**

Direct requests for enhancing capabilities is another common request by customers. As component technologies improve we can often help our customers do more such as increasing process throughput by upgrading power supplies for higher coating rates. Retrofitting new improved process control technologies like the latest quartz or optical monitoring technologies for more accurate layer termination can help customers realise new processes that they couldn't achieve before, improve process repeatabilities where yields are sensitive or simply save money.

### Customised Retrofits

**Reason 3**

Then there are also customer specific retrofits like special tooling designs unique to their own substrate geometries or process requirements. Other examples could be handling conversions from 6 to 8 inch and so on offering customers flexibility to swap between different substrate sizes easily in their daily production.

"Retrofits offer huge potential for enhanced capabilities and improving output"

### Extending working lifetimes and enhancing capability

You can find more information out at
**www.evatecnet.com/service/retrofits-upgrades**

You can find more information out at
**www.youtube.com/watch?v=okXh4ast05A**



### How about new ideas for retrofit services?

We are always looking at new ways of helping customers. One new area is in the field of obsolescence where its often impossible to find replacement units. With Evatec's so called "golden units service" customers can loan parts in an emergency case against a fee while their retrofit is being prepared The unit is then returned to us so we can help other customers if they run into the same situation.

### How does the retrofit ordering process work?

Prior to every retrofit our ideal process involves screening and mirroring the actual situation of the complete customer system with a tool audit executed by a Field Service Engineer. Even more helpful is a full "health check" to recognize further weaknesses and the improvement potential of the system as a whole.

Once the costs and scope of retrofit are confirmed including any tests which need to be conducted on completion of installation by the Evatec engineer an order can be placed by the customer. Our order processing groups will need to check, systemize, and confirm it before the Evatec project leaders responsible manage the project until installation is completed on the customers system. There are many different internal stages of the project including "kick off", engineering, initial procurement, parts receipt, assembly and packing, creation of documentation including any new schematics etc, before shipping and installation is arranged often in collaboration with our local sales and service organization.

### What are the biggest challenges you face in your daily business?

The demand for thin film coating capacity has grown dramatically over the last few years. Of course, this is very good for our business as we deliver new tools but it also drives the demand for retrofits as customers look to their existing tools and how they can maximize benefits more quickly than waiting for delivery of a new tool.

The COVID pandemic created huge challenges for all, but often also made the retrofit process more challenging with difficulties for access on site for surveys, tool health checks or installation work. Limited availability of electrical / electronic components and raw material as well as limited manufacturing capacities or unexpected delays on the supplier side also pushed out lead times for retrofit projects. We certainly need to avoid uncomfortable situations where we start the retrofit installation and then sudden / unexpected issues occur because the preparation with pre retrofit audit was not completed as we want. This is especially true for some of the oldest systems with unknown condition.

### Is there anything else you would like to share with our readers?

More than anything we would like to encourage and support our customers in their planning. With delivery issues at some suppliers our customers are starting to recognize the importance of advance planning of retrofits rather than waiting until the tool is down. We know our customers are all busy with day-to-day things but our job is to help them understand the cost savings they can make and budget. That helps them avoid not just a short term down time while we search for parts but avoid much more costly longer downtimes of potentially weeks because parts are obsolete and no replacement is available. ◻

# ADVANCED PACKAGING NEWS



“Heterogenous Integration and High Performance Computing call for new packaging designs and disruptive technologies. Chiplets are now being adopted to reduce the complexity of monolithic SOCs driving innovation in growing fields of packaging technologies, such is thermal interface materials, high density substrate technologies and fanout packaging. Panel-level packaging is finally taking off with multiple pilot lines already producing first products like application processors in high volume. Here at Evatec we continue to focus on thin film production solutions for such high-end packaging technologies. Who said Packaging is *"just wrapping plastics around a semiconductor die"*?... well definitely not me!”

**Ralph Zoberbier**
Head of BU Advanced Packaging

# CHIPLETS AND THE NEW ERA OF ADVANCED PACKAGING

***E. Jan Vardaman*, President and Founder, TechSearch International Inc. reviews the state of play and the challenges ahead.**

*Image: AMD 3D V-Cache™*
*Courtesy of: AMD*

>>>>>

As the industry enters the new era of heterogeneous integration, advanced packaging in the form of chiplets is becoming increasingly important. An increasing number of companies are turning to chiplets to achieve the economic advantages lost with expensive monolithic scaling, ushering in a new era of smart packaging. A chiplet is not a package, but it is a new approach to system, package, and chip design. There are many package options that can be adopted and careful consideration is required to select the most appropriate options for the application. Options include the emerging 3DIC format with mircobumps or hybrid bonding, laminate substrate package, fan-out on substrate, and silicon interposer. Challenges include design, test, assembly and thermal management.

## What is a Chiplet and what are the advantages?

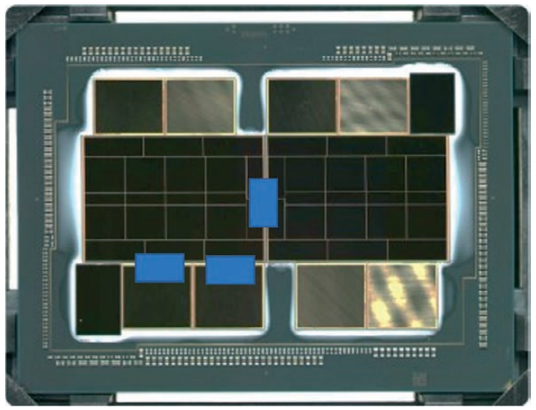
A chiplet is a functional circuit block and includes reusable IP blocks. A chiplet is a physically realized and tested IP with a standard or proprietary communication interface between IP blocks. A chiplet functions with other chiplets, so the design must be co-optimized and the silicon cannot be designed in isolation.

There are numerous advantages with the use of chiplets. AMD indicates that the major drivers for its adoption of chiplets include rising manufacturing cost for large die, increased cost of mask sets, increased complexity of design rules in leading-edge nodes, and architectural challenges of meeting relentless demand for increased computational power. It is also possible to have higher core counts and therefore higher performance than with a monolithic design.  Cost savings at the die fabrication level can be obtained by partitioning die and only fabricating the logic functions on the most advanced nodes where needed most. Smaller die also result in higher yield per wafer, resulting in cost savings. Binning the chiplets provides an opportunity to optimize performance even further. There is a trade-off of increased cost at the packaging and assembly level. Additional costs with chiplets include increased area for interfaces, a more complex design, and often a more expensive package. However, the benefits outweigh the costs.

One of the greatest challenges is how to connect chiplet IP blocks to communicate with each other. There are many different interface options for chiplet communication. There is no single standard die-to-die interface solution in the market today. Many are proprietary, but several organizations are developing open standards. The full potential of chiplet design will not be reached until standards are established.

AMD's proprietary interface architecture is called Infinity Fabric (IF). It has been described as a superset of Hypertransport allowing for fast connectivity between different chiplets. The interface connects CPU blocks to each other and can be used to connect GPU blocks. AMD has introduced multiple generations of server and desktop products using chiplet designs [1].



| Attribute | PVC 2T |
|---|---|
| D2D Pitch | 36µm |
| Top Die Count | 20 |
| Max Top Die Size | 41mm² |
| Base Die Size | 650mm² |
| EMIB Pitch | 55µm |
| Core Pitch (min) | 100µm |
| Memory (HBM) | 8x (8Hw/BSM) |
| Package Size | 77.5 x 62.5mm |
| EMIB Count | 11 |

*Source: Intel*


*AMD INSTINCT™ MI200 OAM Series, Courtesy: AMD*

Intel has introduced Foveros technology as a chiplet solution in which a logic die fabricated on an advanced 10nm node is connected to a base die containing I/O and other functions. The base die is fabricated in a less advanced 22nm node. Intel refers to chiplets as tiles. Intel's Embedded Multi-Die Interconnect Bridge (EMIB) was developed so that the high-density connection is placed only where needed, between the die that need to communicate with chiplets such as a logic die, transceivers, and HBM. With EMIB the substrate supplier places a high-density silicon bridge in a laminate substrate. With Intel's new GPU, Foveros tiles and HBM stacks are connected using EMIB. Intel refers to this as co-EMIB [2]. Intel's Ponte Vecchio uses a combination of Foveros and its Embedded Multi-Die Interconnect Bridge (EMIB). Two Foveros 3D configurations are in the center, plus eight HBM stacks, and two additional chips, connected with 11 silicon bridges in the EMIB. Intel will use its modular die fabric (MDF) proprietary interface for its first CPU server for datacenters.

Intel offers its AIB, a die-to-die PHY level standard royalty free. Open Domain-Specific Architecture (ODSA) has introduced Bunch of Wires (BoW). A new standard interface for chiplets, Universal Chip Interface (UCIe) is being proposed by the UCIe Consortium with members including Intel, AMD, TSMC, Microsoft, Meta, Google, Qualcomm, and ARM.

## Chiplet Package Options

A chiplet can be created by partitioning a die into functions and is typically attached to a silicon interposer or organic substrate today, but new options are emerging such as advanced fan-out, RDL interposer, embedded bridges, and 3D stacking. The close cooperation between all segments of the industry, EDA tool vendors, IC designers, third party IP providers, foundries, and OSATs will help drive the growth of chiplets into a wide range of applications.

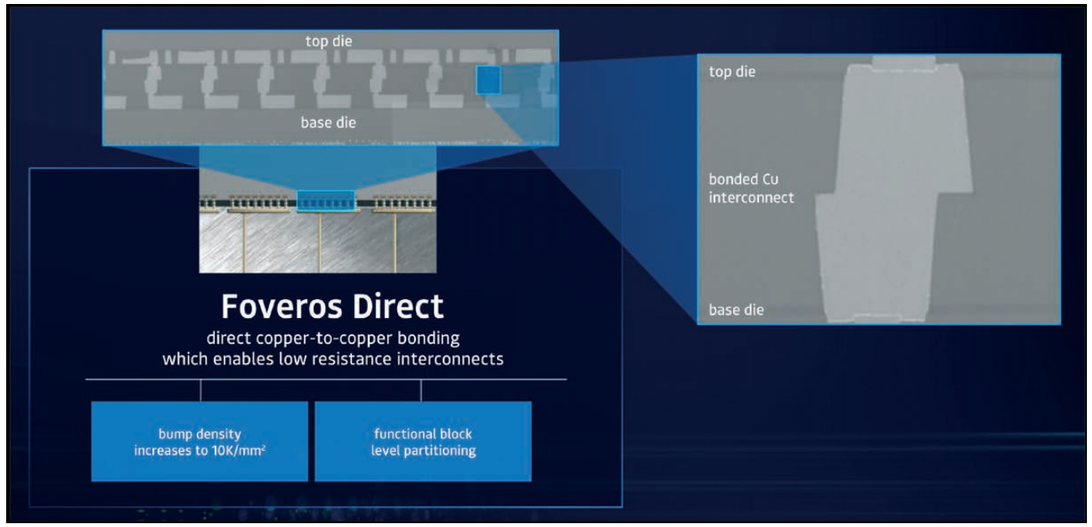
## Laminate Build-up Substrates

AMD's server, desktop, and gaming products use a laminate build-up substrate with fine features to support their chiplet designs. Intel's Foveros technology with microbump connections between the chiplets (called tiles by Intel) uses a laminate substrate to complete the package.

## Silicon Interposers

Silicon interposer with their ultra high-density connections can support chiplet designs. Xilinx, now part of AMD, continues to use a silicon interposer for its high-end FPGA products that are fabricated in slices. Marvel will introduce a chiplet design for network switch applications using a silicon interposer.

>>>>>




*Source: Intel*

## Fan-out

Companies including ASE, Amkor, JCET, SPIL, Tongfu Microelectronics, and TSMC have introduced fan-out on substrate options for chiplets. TSMC has demonstrated a 51mm x 42mm area with five redistribution layers (RDLs) on a 110mm x 110mm substrate. A 36µm die-to-die I/O pitch has been demonstrated [3].

Companies have also introduced fan-out options with and embedded bridge. The embedded bridge provides the potential for a reduction in the number of RDLs and a more relaxed feature size, resulting in higher yields. AMD's INSTINCT MI200 Series, used for machine learning, is packaged by an OSAT using Elevated Fanout Bridge (EFB) technology. GPU chiplets are connected to the HBM using a silicon bridge embedded in the RDL. The package contains two fan-out modules. Each fan-out module contains one AMD CDNA™2 die (chiplet) and four stacks of HBM2E for a total of 2 CDNA™2 die and 8 HBM2Es. The two fan-out modules are attached to the laminate substrate.

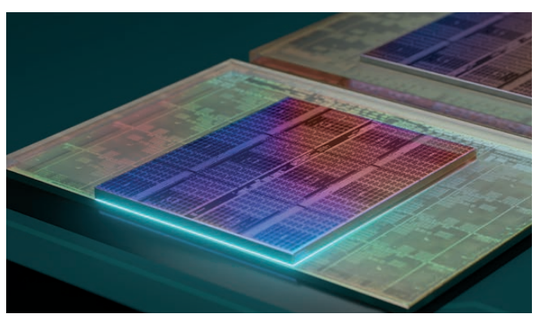


*Image: AMD 3D V-Cache™*
*Source: AMD*

## 3D IC with Hybrid Bonding

TSMC has shown that 3D solutions such as its SoIC™ using hybrid bonding to connect pads without bumps result in higher interconnect bond density. This allows the chip designer flexibility and extensibility on designing a new chip and new system device, adopting the most advanced integration technology for cost and performance advantages. Electrical resistance is lower because there is no solder bump. Lower insertion loss is also reported. High-quality signal integrity and power integrity with low RC delay and low IR drop are also reported. Energy consumption/bit is lower (as measured in pJ/bit) and thermal resistance is lower. This means less energy is required to move data around. With a fixed power envelope, less energy spent per bit means that more bits can be transferred or that the saved energy can be spent on other resources. AMD V-Cache™ using TSMC's SoIC™ technology is in production for server, desktop, and gaming products. A laminate substrate is used for the package. TSMC explained the advantages of a 3D structure with hybrid bonding over a side-by-side chip layout on a silicon interposer or 3D stacking with microbumps for its SoIC™ process (see table page 23).

## Intel's Foveros Direct

Intel is developing a 3D hybrid bonding process for its Foveros technology. The focus is on sub-10µm pad pitch. In the development of its hybrid bonding process, Intel notes that there are new requirements on the bonding layer, die properties such as flatness, and tolerance to process temperatures. Design considerations include the need to consider the impact of top layer passives such as high-speed signal routes, inductors, and transforms due to increased coupling of the die (due to the proximity of the die surfaces).

**SoIC™ Compared to 2.5D and Conventional 3D IC**

| | 2.5D | Conventional 3D IC | SoIC |
|---|---|---|---|
| Interconnect | µbump + BEOL | µbump | Bumpless |
| Chip distance | 100 µm | 30 µm | 0 |
| Bond pad pitch | 36 µm (1.0X) | 36 µm (1.0X) | 9 µm (0.25X) |
| Speed | 0.01X | 1.0X | 11.9X |
| Bandwidth density | 0.01X | 1.0X | 191.0X |
| Power dissipation | 22.9 | 1.0X | 0.05X |

*Source: TSMC*

IBM Research is working to develop hybrid bonding for future products. 3D chiplets will be stacked using nanosheet logic die stacking. Nanosheet refers to the silicon generation that follows FinFET. The 3D stack will be mounted on a high-density laminate substrate. Samsung Electronics is developing a 3D hybrid bonding process. The focus is on logic such as CPU, GPU, and NPU plus SRAM (cache memory).

While hybrid bonding offers many advantages, there are also challenges. Samsung is focused on addressing challenges such as Cu pad surface control, cleanliness, pad alignment accuracy, bonding temperature, metrology, and developing an integrated bonding/assembly system [4].

## Promises and Challenges

There are tremendous advantages with the adoption of chiplets, especially using 3D hybrid bonding. 3D hybrid bonding will also offer much greater advantages than could ever be reached with monolithic scaling. The adoption of chiplets will have a similar impact on the industry as the move from peripheral chip layout to area array. The chiplet strategy is not without its challenges and associated cost. Packaging chiplets is expensive. Co-design is a must. Chiplet IP blocks must be able to communicate with each other. Standard interfaces are needed. Careful thermal analysis is important, especially with 3D stacking. Hybrid/bumpless bonding requires a clean surface for bonding and a clean environment. Particles will result in failures. New test and inspection methods are needed. These challenges are not insurmountable and an increasing number of chiplet solutions are entering the market with a growth rate of 76% expected over the next three years. ◻

**E. Jan Vardaman** is president and founder of TechSearch International Inc., which has provided market research and technology trend analysis in semiconductor packaging since 1987. She is the author of numerous publications on emerging trends in semiconductor packaging and assembly. She is a senior member of IEEE EPS and is an IEEE EPS Distinguished Lecturer. She received the IMAPS GBC Partnership award in 2012, the Daniel C. Hughes, Jr. Memorial Award in 2018, the Sidney J. Stein International Award in 2019, and she is an IMAPS Fellow. She is a member of MEPTEC, SMTA, and SEMI. Before founding TechSearch International, she served on the corporate staff of Microelectronics and Computer Technology Corporation (MCC), the electronics industry's first pre-competitive research consortium.

1. S. Naffziger et al., "Pioneering Chiplet Technology and Design for the AMD EPYC and Ryzen Processor Families," *2021 ACM/IEEE 48th Annual International Symposium on Computer Architecture*, June 2021, pp. 57-70.

2. E. J. Vardaman et al., "Quantifying the Impact of Heterogeneous Integration: Chiplets and SiP," TechSearch International, Inc., February 2021.

3. Y. Chiang et al., "InFO_oS (Integrated Fan-Out on Substrate) Technology for Advanced Chiplet Integration," *Virtual Electronic Components and Technology Conference*, June 1 - July 4, 2021, pp. 130-135.

4. S.W. Yoon, "Challenges and Opportunities of Packaging FAB Near the End of Moore's Law," *IMAPS*, October 2021.


# TOWARDS PERFECTION IN ADVANCED PACKAGING WITH THE NEW HEXAGON

**Building on the success of the existing system, the new HEXAGON maintains the existing strengths of proven and reliable processes, high throughput and then offers significant improvements and innovations in the areas of process capabilities, throughput, uptime, accessibility and serviceability. Product Marketing Manager *Markus Frei* tells us more.**

### Why did Evatec launch a new HEXAGON?

The existing tool concept with its Indexing system was well qualified and considered by many as the benchmark in the Advanced Packaging industry for seed layer processes, but we recognised that market requirements were changing.

We wanted to deliver a platform that could address both the need for more ambitious $R_c$ requirements and the continuous push to lower Cost of Ownership (CoO). We also wanted to implement improvements based on customer feedback and provide the most robust platform in the industry.

Our goal was to bring the HEXAGON platform to the latest state of the art technology level and provide a sound solution to our customers that meets their long term process roadmap requirements.

### What are the main benefits of the new system?

The new generation tool offers a number of benefits for our customers:

- Best Rc in industry
- More uptime, lower scheduled maintenance time
- More reliability and extremely safe wafer handling
- More throughput
- More process flexibility
- More possibilities
- More accessibility

Bringing all these things together results in higher efficiency and overall CoO.

### What system aspects were essential to keep?

The handling performance and speed at the heart of the existing tool was something we very much wanted to keep. HEXAGON handles Si, EMC and Glass substrates of different sizes with ease. That also meant keeping the right degassing method.

Our second generation atmospheric high pressure degasser provides excellent degassing performance without cross contamination.

The proven indexer concept then transfers the substrate through the individual process stations with unbeatable speed to improved process modules delivering best process performance at lowest cost.

>>>>>

**About the author:** Markus Frei originally trained as an engineer and has over 20 years experience in vacuum and thin film technology. As product manager he gained 10 years know-how working with the unique indexing system at the heart of HEXAGON before he joined the Advanced Packaging group as Product Marketing Manager in 2021.

## What are the biggest changes?

Here are some of the biggest changes that we have made:

### New Transfer Chamber (VIN6)

The new VIN6 comes with a new indexer drive. Although new to HEXAGON, it is already field proven in more than 2000 systems. The improved "on the fly" function brings even more wafer transport safety to the already existing excellent handling performance. The VIN6 accepts 5 process chambers tailored to the needs of Advanced Packaging with an optimized load lock which provides a fast wafer exchange.

### New Atmospheric Front End Module (AFEM)

We have integrated new wafer mapping and automatic home position detection that detect critical situations in the AFEM such as cross-slotted wafers, excessive wafer bow on FanOut, and double-loaded wafers. In combination with the new AWC (automatic wafer centering) function the wafer will be brought safely to the load lock.

### Enhanced process technology

**Degas:** Atmospheric degas is key! Giving enough time at moderate temperature without any cross contamination is a must for processing of wafers with high organic load and especially for FanOut. Degassing at a temperature of around 120°C with a good temperature uniformity ensures even and proper degassing independent of the emissivity mix on the substrate.

**ICP:** The proven SEQ 300 etch cathode offers improved uniformity with a newly designed chuck. Evatec's patented insitu pasting solution is also available as an option. Adding in a new etch chamber design and the longest "Kit life" in the industry results in the best etch performance ever.

**PVD:** Our well known ARQ 310 provides efficient deposition. Using only 400mm diameter long-life targets together with our uniformity compensation over target life we reach a new benchmark for target lifetimes but also for CoO.

### New services system

The media distribution system is designed into the base pedestal, resulting in easy installation, good access, and easy maintenance.

### New control system

A new control system comes with the proven Siemens TIA portal and state of the art GUI giving you direct access to your hardware components like drivers for maintenance and service. No additional software or devices are needed.

For those already familiar with Evatec's latest CLUSTERLINE® generation which uses the same software platform, minimum cross training will be required for operation, maintenance and service. New features eliminate or reduces complex tasks like teaching and calibration and other improvements make the system easier to work with.

### Unified platform concept

The approach taken in the newly designed HEXAGON and CLUSTERLINE® platforms brings benefits for long term field support too. Modular and standardized design leads to fewer individual parts, the smart modules use distributed I/O functions, and a powerful Profinet bus simplifies the system, increasing uptime and productivity. Optimised architecture of the system results in faster manufacturing times and reduced ramp up-time to production. Footprint of the system is reduced taking up less costly cleanroom space and the system is designed to meet the newest ISO 14001 environmental standards, conserving water usage and energy.

### Welcome to the new HEXAGON

We are excited to see the performance of our system with an even safer level of wafer handling to protect the high value of our customers' wafers.

Combined with the benefits from higher productivity, higher throughput, reduced maintenance time and easier support during its working life, the new HEXAGON system really does set new standards for Advanced Packaging applications.


### The new HEXAGON improvements at a glance

- New direct servo drive system
- New standardized 3 wide AFEM
- New control system
- Improved throughput
- Insitu pasting available
- Improved etch uniformity
- Modified Atmospheric Batch Degasser
- Optimized Loadlock
- Incorporating automatic wafer centering, reduced volume
- New process modules
- Higher pumping speed
- Improved system service and maintainability

## Facts and figures

**2000**
The new VIN6 Transfer Chamber comes with a new indexer drive already field proven in more than 2000 systems.

**100**
Enjoy throughputs of >100 wafers per hour according to process.

**5**
Configure up to 5 process modules for etch and deposition processes.

Find out more information at
**evatecnet.com/products/hexagon**

# LOW TEMPERATURE PVD DEPOSITION OF LOW STRESS SiN AND SiCN FILMS FOR HYBRID BONDING APPLICATIONS

Intel's ***Dr. Xavier Brun***, and Evatec's ***Dr. Patrick Carazzetti*** and ***Ewald Strolz*** investigate the feasibility of high quality low stress SiN and SiCN film deposition on Evatec's CLUSTERLINE® at low temperatures without adversly affecting tool productivity. Results confirm the possibility of achieving good uniformities (<3% 1σ) for up to 2.0µm films, and optimization of SiN film stress (100MPa) independent of film thickness.

## Introduction

As transistors' density grows with each new Silicon node, the package technology needs to scale accordingly. New challenges in packaging arise as the pitch of the first-level-interconnects (FLI) shrinks below what can be achieved with solder joints. Hybrid bonding, including dielectric bonding plus direct Cu-Cu bonding, is a promising solution, but faces significant integration challenges due to the stringent requirements to enable a high yield bonding process for dielectric and Cu interfaces while maintaining low processing temperatures to ensure package integrity. Many studies have demonstrated the benefit of silicon carbonitride (SiCN) dielectric compared to silicon oxide ($SiO_2$) for decreasing the bonding temperature, specifically reducing the annealing temperature below or equal to 250°C. Unfortunately, these studies have leveraged plasma enhanced chemical vapor deposition (PECVD) which requires high deposition temperature (i.e., 370°C) and precursors. In addition, these films necessitate pre-bonding densification above deposition temperature to prevent voiding at the bonding interface [1-3]. PVD was recently reported to be a superior alternative method for silicon nitride (SiN) dielectric deposition for bonding applications with low deposition temperature, not requiring densification pre-bonding, and achieving comparable bond strength with low post-bonding annealing temperature [4].

Significant work on PECVD SiN and SiCN deposition of thin films on silicon substrate semiconductor device has been reported in the literature [5], of particular interest [6] reported the impact of substrate temperature for SiCN PECVD on film growth and composition. High substrate temperatures (>400°C) are needed to ensure mass transport mechanism for film deposition in addition to limiting the oxygen content in the film [6]. However, limited work has been done on the use of PVD for the dielectric film deposition process for advanced packaging applications, particularly looking at ensuring the low temperatures required for device integrity (<250°C). To this end, a set of low temperature PVD depositions of SiN and SiCN thin films on p-type (100) Silicon substrates is presented here. The deposition temperature as a function of the deposition time is characterized. In order to provide insights of handling flexibility, two hardware configurations have been tested depending on if contact on non-deposition side of the substrate is allowed. In both cases, an optimized process is presented to minimize the substrate temperature. In order to mitigate the impact of stress induced warpage at wafer level and its impact on downstream applications, the deposition process was optimized to target minimum film stress and make the stress essentially independent of the film thickness. Therefore, the film stress is characterized as a function of the film thickness. To comprehend a wide range of packaging applications, the low temperature deposition of SiN on epoxy mold compound (EMC) is also presented. The quality and hermiticity of the deposited films have been assessed on both inorganic and organic substrates with accelerated temperature and moisture bake experiments.



This study presents a comparison of SiN and SiCN thin films sputtered on a high-volume manufacturing CLUSTERLINE® PVD platform. Of particular interest is the limitation of the deposition temperature without adversely impacting tool productivity (e.g., the run-rate). The impact of the film thickness on stress and warpage is reported. Although this study focuses on blanket films, fundamentals are presented to define the best integration for packaging applications such as hybrid bond dielectric preparation for FLI bonding, or direct bond dielectric preparation to combine heterogenous materials (e.g., integrating a Si passive interposer on backside of an exposed die package for improved thermal performance).

## Experimental Method

### Film deposition and characterization

Magnetron sputtering is a well-established PVD technology in microelectronics manufacturing and advanced packaging for the deposition of metal and dielectric films. The main benefits of magnetron sputtering include high deposition rates, excellent thickness uniformity, tight defect control and low deposition temperatures compared to CVD and PECVD counterparts. In this work, amorphous films of silicon nitride (a-SixNy) and silicon carbonitride (a-SiCxNy) were deposited on bare silicon substrates by DC magnetron sputtering in a mixed atmosphere of nitrogen and argon. The main hardware features of the process modules, as well as the key process conditions are summarized in Table 1. A polycrystalline Si target with 400mm diameter was used to sputter SiN in a CLUSTERELINE® 300 high-volume manufacturing tool configured for 300mm wafer sizes. The deposition conditions of the SiN best-known method (BKM), such as power density, $N_2$/Ar gas ratio and process pressure are reported in Table 1. Two important tuning knobs have been identified to reduce the stress of SiN films. These are the use of DC power in pulsed mode, in combination with the increased process pressure obtained by pump throttling. The SiCN films were prepared on a CLUSTERLINE® 200 platform configured for 200mm wafer sizes. This tool was equipped with a 300mm diameter powder pressed SiC target, with a 1:1 silicon/carbon ratio. The process conditions of the established SiCN BKM are also reported in Table 1.

Both of the CLUSTERLINE® platforms used are both multi-chamber PVD tools with up to six process modules clustered around a central vacuum transport section. This configuration allows execution of a sequence of processes in different modules without breaking vacuum. The CLUSTERLINE® 300 configured for BSM processes, uses recessed chucks to prevent direct contact of the device side of the wafer with the pedestal surface. Only the wafer perimeter rests on a metal supporting ring located around the chuck top. The additional requirement for full face deposition in BSM applications forbids the use of any mechanical fixation of the substrate edge. Therefore, the substrate can only dissipate the heat (generated by the film growth) through radiation. To favor such heat dissipation so that the increase of temperature during deposition is limited, a simple approach was followed: alternating deposition steps with cooling steps. The implications of such "split process" on the wafer temperature and the corresponding run-rate will be discussed in Section III. Contrary to the CLUSTERLINE® 300, the CLUSTERLINE® 200 was not bound by a BSM hardware configuration. Instead, the PVD module used in this work was equipped with a clamping setup, that mechanically fixates the wafer edge by the mass of the clamping mask. As a result, the entire wafer surface is in contact with the water-cooled pedestal. Moreover, Ar gas flows beneath the substrate through a dedicated inlet at the center of the chuck and it is distributed over the entire wafer surface by a network of grooves thereby promoting efficient cooling by conduction.

In advanced packaging applications, the common practice to pre-treat a substrate prior film deposition consists of a sequence of degas and soft-etching processes [7]. Degas is applied to eliminate surface moisture from the organic films and substrates by heating the wafer typically up to 120-150°C. The subsequent soft-etching takes place in a dedicated Inductively Coupled Plasma (ICP) Etch module. Here, the bombardment of the substrate by low-energy Ar plasma effectively eliminates surface contamination and native oxides, thereby enhancing adhesion of the subsequent PVD film.

| Hardware and Process Conditions | Film / PVD System | |
|---|---|---|
| | SiN / CLUSTERLINE® 300 | SiCN / CLUSTERLINE® 200 |
| Target | Si polycrystalline (disc Φ=400mm) | SiC powder pressed (1:1 ratio, disc Φ=300mm) |
| Power source | Pulsed DC (frequency=350kHz; pulse-off time=1100ns) | Continuous DC |
| Power density [W/cm²] | 6.37 | 4.95 |
| Gas ratio $N_2$/Ar [-] | 1.0 | 1.2 |
| Sputtering pressure [mbar] | $1.3e^{-2}$ (pump throttled) | $9.7e^{-4}$ |
| Pedestal type | Clampless, recessed chuck top, PCW cooled pedestal | Clamped, flat chuck top with back-gas inlet, PCW cooled pedestal |
| Pre-treatment process | Radiation degas (load-lock) and ICP-Etch | ICP-Etch |

*Table 1: Hardware configuration and process conditions used to sputter deposit SiN and SiCN films.*

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## Low temperature SiN reliability assessment

In this section, the focus is on reliability of the low temperature deposited films. SiN films were deposited on both inorganic materials, i.e. p-type (100) Silicon substrate, and organic materials, such as EMC on a Si substrate, to comprehend a wide range of packaging applications. All the samples were processed using the same low temperature process described above on the 300mm tool. To improve the adhesion to the organic material interface, this study includes understanding the impact of an ICP-etch step pre-deposition. To envelope a range of mold materials available, two different mold compounds were compared side by side. As shown in Table 2, liquid and granular EMC have different mechanical properties particularly Young's Modulus and Coefficient of Thermal Expansion (CTE).

| | Sample | | Mechanical Properties | |
|---|---|---|---|---|
| | Stack | Interface Material | CTE [ppm] | E [GPa] |
| Inorganic | 1.5µm SiN<br>775µm Si | Silicon | 2.3 | 170 |
| Organic | 1.5µm SiN<br>100µm Mold<br>775µm Si | Granular EMC<br>Liquid EMC | 5.0<br>16.0 | 20<br>9 |

*Table 2: Material properties - SiN reliability experiments*

After deposition, standard diamond dicing was used to singulate the wafers into samples that were then submitted to Temperature/Humidity plus preconditioning (JEDEC standard J-STD-020 [8]) and extreme preconditioning for margin assessment and HTSL/Bake (JESD22-A103 [9]) to accelerate SiN de-lamination and dielectric cracking failure modes. The cracking in SiN results from moisture assisted crack growth propagation. Macroscopic and microscopic inspections were performed to detect the presence of defects such as SiN cracking, flaking, fringing, etc., both post singulation and post temperature/humidity exposure.

## Results and discussion

### Films performance summary

In this experimental study, various SiN and SiCN films with thickness ranging from 100nm up to 2.0µm were sputtered on bare silicon wafers and were characterized without performing any densification or annealing. Spectroscopic ellipsometry (Woollam M-2000) was used to measure film thickness, refractive index (n) and extinction coefficient (k). In-wafer statistical data was collected using a 49-points circular pattern with 6.0mm edge exclusion. The film uniformity is an important metric to characterize the quality of a deposition process. The uniformity criteria adopted here is "1σ", which is defined as standard deviation of the thickness distribution divided by the average. The film density is calculated based on the mass difference of the wafer pre- versus post-deposition. Table 3 summarizes data measured on 2.0µm-thick films of SiN and SiCN. The obtained 1σ uniformities are below 3% for both films. These values can be considered satisfactory and show that the PVD processes developed are suitable for depositing high-quality films at least up to 2.0µm with deposition rates in excess of 20.0Å/sec. We measured a SiN refractive index of 2.11. This can be compared to published n values ranging from 3.18 to 2.1 with N/Si ratio increasing from 0.31 to 1.5 [10]. The measured density of the 2.0µm SiN film is 2.7 ±0.05 g/cm$^3$. This value matches well with published data of 2.8 g/cm$^3$ for a film with N/Si ratio of 1.1 [11] and 2.28 to 2.97 g/cm$^3$ depending on the deposition pressure [12]. The refractive index of the SiCN film is 2.29 and the corresponding density is 3.5 ±0.5 g/cm$^3$. Published data show a direct relationship between increase in the nitrogen content in the film and the concomitant increase of both density and refractive index. Inoue et al. [3] reported a refractive index of 1.95 and a corresponding density of 1.98 g/cm$^3$.

| Performance | Film / Substrate | |
|---|---|---|
| | SiN / 300mm wafer | SiN / 200mm wafer |
| Deposition rate [Å/sec] | 20.71 | 23.68 |
| Thickness uniformity, 1σ [%] | 2.97 | 1.62 |
| Refractive index, n @633nm [-] | 2.11<br>(3.18-2.1 in [10]) | 2.29<br>(1.95 in [3], and 2.1-2.3 in [13]) |
| Density as-sputtered [g/cm$^3$] | 2.7 ± 0.05<br>(2.8 in [11,12]) | 3.5 ± 0.5<br>(1.98 in [3]) |

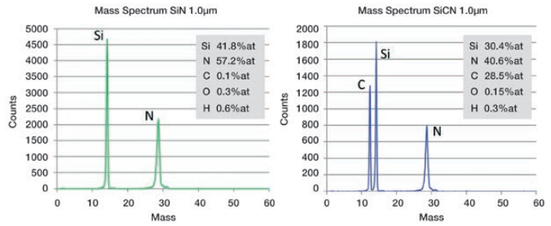
*Table 3: Properties of 2.0µm SiN and SiCN films*

### Elastic recoil detection analysis (ERDA)

ERD analysis uses high-energy heavy ion beam to determine the elemental depth concentration profiles in thin films [14]. In this work, the analysis was performed on selected samples of 1.0µm SiN and 1.0µm SiCN by 13 MeV 127I Heavy Ion ERDA. The elemental composition was retrieved from the bulk of the film at a depth of about ~30-150nm so that the surface contamination is not considered. ERD spectra of SiN and SiCN films are displayed in Figure 1. The empirical stoichiometry formulas reported in Table 4 were established based on the elemental composition normalized to Si. In the case of SiN, a normalization factor of 3 was used; whereas, in the case of SiCN the normalization factor was 1.



The ratio of Si to N in the silicon nitride film is 3 to 4.1, indicating that a nearly stoichiometric Si3N4 is formed. The other elements in the measured mass spectrum: C(<0.1%at), H(<0.6%at) and O(<0.3%at) are present as impurities. Published research shows that the N/Si ratio can be tuned between 0.56 (under-stoichiometric) and 1.33 (stoichiometric) depending on the N2/Ar ratio in the process atmosphere [15]. The ratio of Si to C in the SiCN film is 1 to 0.99, which validates the nominal composition of the target. Beside the target elements and nitrogen, experimental data show a very minor content of H (<0.3%at) and O (<0.15%at). In the linear scale spectrum such low content of H and O is not visible. The composition of SiCN produced in this work is richer in nitrogen and it is substantially hydrogen-free compared to the published data [3].




| Film | Empirical formula | | | | |
|---|---|---|---|---|---|
| | Si | C | N | H | O |
| SiN | 3 | 0.006 | 4.1 | 0.024 | 0.041 |
| SiCN | 1 | 0.99 | 1.40 | 0.01 | 0.005 |
| SiCN [3] | 1 | 0.79 | 0.75 | 0.62 | 0.003 |

*Table 4: Empirical stoichiometry formula of sputter deposited SiN and SiCN films derived from ERD analysis*

### Wafer temperature and stress vs. film thickness

The maximum temperature of the wafer during deposition was measured using thermal labels (Celsistrip® Spirig – Switzerland). These labels use a scale of markers reacting at a progressively higher temperature in steps of 5-6°C, which represents the measurement resolution. Each marker turns to black when triggered, thereby indicating the peak temperature reached during process. In our tests, the thermal label was placed on the deposition side at the center of each monitor wafer. Figure 2 compares the process temperature versus the film thickness for SiN films produced on CLUSTERLINE® 300 (split deposition process), and SiCN films produced on CLUSTERLINE® 200 (single step deposition process).

The strategy of splitting the deposition process alternates deposition steps of 100nm (equivalent to a process time of 47.0sec) followed by a cooling step of 60sec. Five different films with thickness ranging from 100nm up to 2.0µm were deposited in this process regime. Prior to PVD, each monitor wafer was pre-treated with degas and ICP-etch, which resulted in a peak temperature of ~150°C. The peak temperature post PVD shows an increase to ~180°C for the 100nm SiN film, up to ~207°C for the 500nm film and then a stabilization to ~228°C for all other thicker films (♦ markers in Figure 2). This behavior indicates the effectiveness of the deposition/cooling regime adopted to stabilize the peak temperature. As a comparison, SiN deposition of 300nm, 500nm run in a single step without cooling reach ~40-50°C higher temperature (▲ markers in Figure 2), and the 1.0µm process exceeded the upper range of 260°C.

SiCN processes run on CLUSTERLINE® 200 indicate a stable temperature of ~100°C, independently from the film thickness (● markers in Figure 2). In fact, it was shown that 100°C substrate temperature was reached already during the ICP-etch prior deposition. This highlights the effectiveness of the hardware setup combining mechanical wafer clamping and active back-gas cooling.

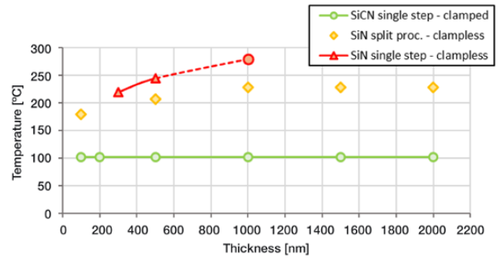



***Figure 2: Peak wafer temperature corresponding to SiN and SiCN films of various thickness processed either in single deposition step, or split process, respectively.***

An additional set of wafers processed with the same condition was used to characterize the residual film stress. The in-plane stress was measured by recording the change of the curvature radius of the substrate induced by the deposition process [16]. The wafer curvature and bow were measured optically with a stress analyzer Tencor FLX-3300-T. The well-known Stoney's formula was used to relate the measured substrate curvature to the residual film stress, σ as:

$$\sigma = \frac{E_s}{6(1-\vartheta_s)} \cdot \frac{t_s^2}{t_f}\left[\frac{1}{R_1} - \frac{1}{R_0}\right]$$

Where Es/(1-$v_s$) is the biaxial Young's modulus of the substrate (180.5 GPa for (100) oriented Si wafers), ts and tf represent the thickness of substrate and film, respectively. R0 and R1 are the curvature radii before and after deposition. The measured stress as a function of the

>>>>>

film thickness are displayed in Figure 3. Both SiN and SiCN films exhibit a compressive stress level, which becomes more moderate as the thickness increases. Particularly, a stabilization is observed when the film thicknesses exceeds 1.0µm. In the case of SiN, a plateau is reached at -65 ±5MPa, whereas the stress of SiCN films levels off around -280 ±20MPa. Residual compressive stress level means that the deposition process has produced a dense and compressed film, which tends to expand in order to relax its internal energy. In this case, the film expansion exerted on the substrate results in a convex warpage [17]. In the worst-case scenario, a highly compressive stress distribution can lead to catastrophic failure mechanisms, such as film buckling, blistering or peeling off. However, the moderate compressive stress of SiN films obtained in this work should not represent concerns of the film integrity, or subsequent integration and device reliability issues. The minimization of SiCN stress can also be investigated by using tuning knobs, such as DC sputtering in pulsed mode and pressure modulation, similarly to SiN. This will be addressed in future work.

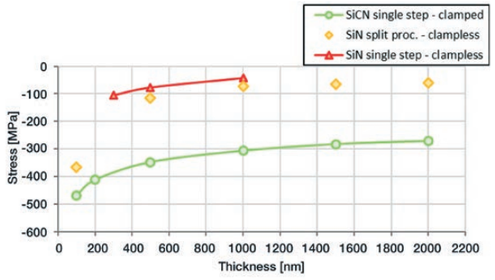



*Figure 3: Film stress a function of the thickness for single step SiCN deposition process, and single step versus split process*

## Run-rate vs. film thickness

In order to keep a viable tool productivity, especially when processing thick films with stringent temperature requirements, it may be necessary to have more than one deposition chambers. This section provides some guidelines to establish the suitable tool configuration based on the required film thickness and the run-rate goal. The run-rate defines the tool output in terms of number of wafers per hour processed from job start to end. Different scenarios have been considered and executed on the HVM platform equipped with one ICP-Etch and up to four PVD chambers. The run-rate figures are reported in Figure 4.a (split deposition process like SiN) and Figure 4.b (single-step deposition).

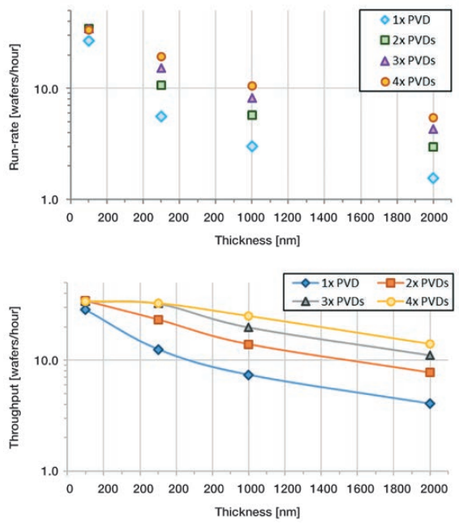



*Figure 4: Run-rate vs. film thickness and number of PVD chambers: (a) SiN split deposition process with cooling steps, and (b) SiCN single step deposition process*

## Stress Test Results

Stress test experiments were performed with low temperature SiN layer singulated samples on two types of EMC and the Bare Si. For the EMC samples, ICP etch was studied to understand its impact on the SiN to EMC adhesion. For each leg, a total of 6 units were used. Table 5 summarizes the reliability results for all the samples. For the silicon samples, no gross delamination was observed on all the conditions. This is because the CTE mismatch between Si and SiN is lower, which leads to lower shear stress at the interface as the temperature changes. Thus, the risk for the interfacial delamination is lower than the one for the organic samples.

| Type | Sample | | Reliability results [# units with delamination/total units] | | |
|---|---|---|---|---|---|
| | Mold type | Pre-Etch | 168hrs 60°C / 60% RH +10x reflow 260°C | 216hrs 30°C / 60% RH + 3x reflow 260°C | 1000hrs 150°C |
| Inorganic | None | No | 0/6 | 0/6 | 0/6 |
| Organic | Granular | No | 6/6 | 6/6 | 0/6 |
| | Granular | Yes | 0/6 | 0/6 | 0/6 |
| | Liquid | No | 0/6 | 2/6 | 0/6 |
| | Liquid | Yes | 0/6 | 0/6 | 0/6 |

*Table 5: Low temperature SiN reliability results*

All the units were also inspected for SiN cracking optically. Only the units with no etch showed SiN cracking for both granular mold and liquid mold, with the latter being less severe (Figure 5). Although Liquid mold having higher CTE mismatch shows better performance than granular, this could be due to its much lower young's modulus and more significant stress relaxation for liquid mold material [18]. Blade dicing impact on SiN was also analyzed side by side for all the samples at time 0 and post reliability test. Si substrate and all organic non-etched samples showed fringes representing SiN delamination at the edge of the sample in Figure 6. Note that no delamination extension was observed post reliability on the Si substrates. A clear benefit was observed with the addition of the etch process for both organic materials. In addition, it was observed that granular mold singulation chipping performance was qualitatively better than the liquid mold material, which could be explained due to its higher hardness or young's modulus.

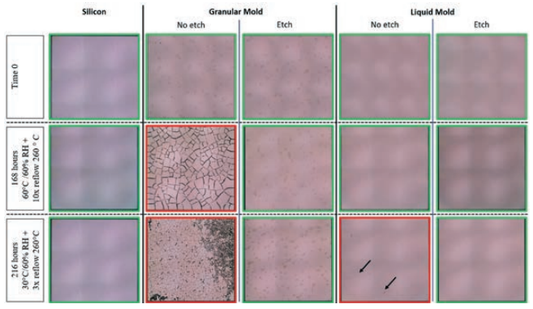



*Figure 5: Low temperature SiN surface macro inspection (3x diopter) on organic and inorganic substrates with and without etch at time 0 and post reliability testing*

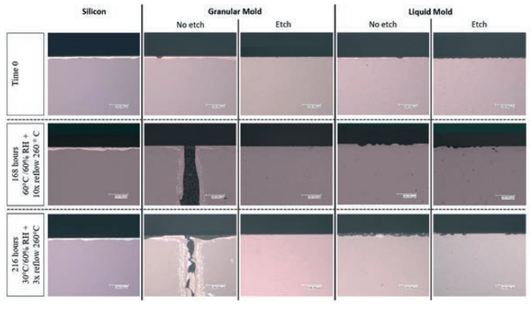



***Figure 6: Low temperature SiN surface and singulated edge micro inspection (20x microscope) on organic and inorganic substrates with and without etch at time 0 and post***

To further investigate the low temperature SiN delamination mechanism, additional inspection was carried for the granular EMC post reliability. Massive cracks in nitride are observed throughout the sample at 20x (Figure 7a). By looking at higher magnification, areas of flaked nitride were observed along with exposed mold (Figure 7b). Exposed mold showed areas of small filler pull out with intact large fillers (Figure 7c). Bottom of flaked nitride was inspected (Figure 7d) and revealed presence of small fillers indicating cohesive failure within the mold. Energy dispersive spectroscopy (EDS) confirmed the presence of mold fillers at the bottom of flaked nitride (Figure 7e).

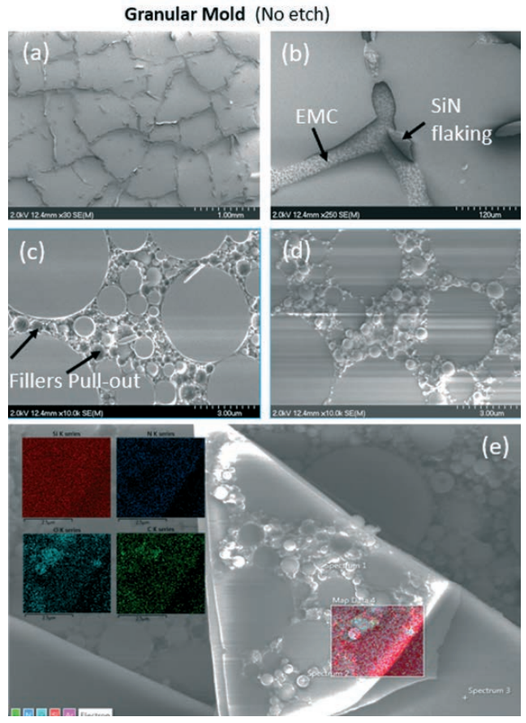



*Figure 7: Low temperature SiN surface inspection (SEM) on granular EMC substrate without etch post reliability. a) Gross SiN cracking observed at 20x, b) Mold exposed and SiN flaking observed at 250x, c) Exposed Mold area without SiN (delaminated area) at 10kx, d) Bottom of SiN (delaminated area) at 10kx, e) EDS analysis on bottom of SiN confirming mold filler pull out*

Although, within mold cohesive failure was observed for granular mold, it is still important to understand the influence of etching. As mentioned earlier, soft etching is generally performed to clean surfaces before deposition. This would not explain the difference in performances between the liquid and granular mold observed in the reliability tests. Therefore, additional characterization with atomic force was performed demonstrating the etch impact on surface roughness. In all cases, etch increased the roughness of the mold compound, therefore, increased the contact area with the deposited nitride. As a result, it provided better mechanical interlocking of the SiN film with the organic material (Figure 8). Interestingly, unetched liquid sample showed higher roughness compared to granular mold that may explain the reliability difference.

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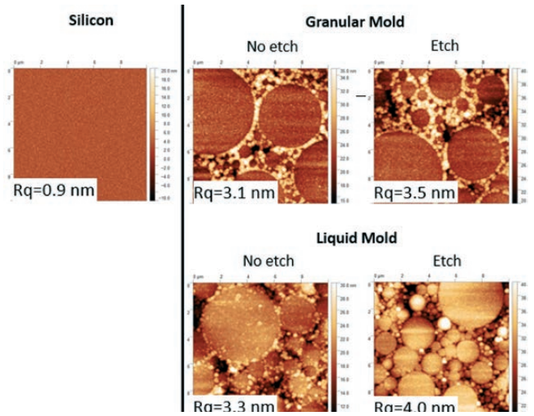


*Figure 8: Low temperature SiN surface roughness measurement (AFM) on organic and inorganic substrates with and without etch at time 0.*

## Conclusion

A low temperature PVD dielectric deposition process has been demonstrated both for SiN and SiCN thin films. This helps Hybrid bonding integration and ensure package integrity by lowering the deposition process temperature. PVD of SiN and SiCN films with good uniformity for up to 2.0µm film thickness was demonstrated. Residual stress was characterized to understand its impact on the wafer warpage. For both dielectrics, above a minimum film thickness, the stress becomes almost independent of the film thickness. The SiN process was optimized to near zero stress (~50MPa compressive) on Silicon substrate, indicating a minimized impact on wafer warpage. The criticality of the substrate cooling was observed. Two different deposition approaches were presented: one by splitting the process with deposition and cooling cycles; the other by leveraging an improved cooling path for the substrate. Both approaches showed effective substrate temperature control, with the later had less impact on the run-rate. Compared to PECVD films, which use precursor gases, PVD films are free of impurities and do not require any densification (annealing). Industry usually requires above deposition temperature densification to prevent voiding at the bond interface. The PVD deposited SiN composition showed low Hydrogen content. The SiCN PVD obtained was Nitrogen rich compared to PECVD films, its chemical composition on Bonding performance will be investigated in the future.

Reliability of SiN was studied on both inorganic and organic interfaces. Films' quality and hermiticity were assessed with accelerated temperature and moisture bake experiments. Adding ICP-etch on EMC before SiN deposition improved film adhesion with an increased surface roughness and samples survived all the stress conditions, while un-etched samples exhibited SiN cracking and delamination.

## Acknowledgement

The authors wish to acknowledge Joel Fischer and Nico Lipp at Evatec for valuable support, and Max Döbeli at ETHZ for ERD analysis. In addition, the contributions of multiple stakeholders within Intel FA and reliability team, Shashank Kaira for the films inspections, Mohit Khurana for AFM characterization, Sarah Wozny and Alan Johnson for their discussions on film reliability.

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## About the authors

**Dr. Xavier Brun**
Xavier Brun is a Principal Engineer and the Director of the Assembly Pathfinding & Prototyping Lab (AP&PL) at Intel Corporation. He is responsible for driving the research and pathfinding efforts for Hybrid Bonding scaling as well as prototyping first-of-kind IPs and demonstration vehicles for Intel's business units, Components Research, and Intel Labs. With over 14 years' experience in packaging, he led the development of EMIB die preparation, temporary carrier solution and backside metallization for Foveros. Xavier received his Ph.D. in mechanical engineering from the Georgia Institute of Technology in 2008, has authored over 15 papers on packaging and has received two Intel Achievement Awards. He currently holds 12 US patents and has over 50 filings.

**Dr. Patrick Carazzetti**
Patrick Carazzetti holds a M.Sc. degree in materials science from the EPFL in Lausanne, Switzerland (2002), and a Ph.D. from the Institute of Microtechnology at the University of Neuchâtel, Switzerland (2006). From 2006 to 2008 he was post-doc fellow at the Laboratory of Microsystems for Space Technologies, EPFL. In 2008 he joined the process engineering group at Oerlikon Systems, and since 2015 he works with the Business Unit Advanced Packaging at Evatec AG. In his role of senior process engineer, his focus is on the development and characterization of sputter deposition and soft-etching processes for various wafer-level packaging applications, such as UBM/RDL, Fan-Out, 3-D packaging and Backside Metallization (BSM).

**Ewald Strolz**
Ewald Strolz holds a degree in electrical engineering from University of applied science NTB in Buchs Switzerland. He has 30 years professional experience in high-tech industry, of which more than 20 years was in semiconductors, holding different positions in engineering, project and product management. As Head of Process Development at Evatec, he is responsible for the process development and application engineering in the Business Unit Advanced Packaging, with focus on sputter solutions for applications like UBM/RDL, Fan Out on wafer and panel level including IC substrates but also sputtered solderable BSM stacks for heat dissipation in heterogeneous integrated packages.

**For more information**

You can find more information out by emailing **ewald.strolz@evatecnet.com**

**Updates**

Results for SiCN films sputtered on 300mm are also now available

# SEMICONDUCTOR NEWS



> We are living in a futuristic world interacting with millions of electronic devices either openly or unknowingly at every single moment. Through our four market segments, Power Devices, Wireless, MEMS and Front End Integration, our goal is to provide the smartest thin film solutions enabling the technologies of today and shaping those of tomorrow.

**Dr. Carlo Tosi**
Head of BU Semiconductor

# FULL STEAM AHEAD

## Welcome to our growing Semiconductor team

**Global mega trends, including the push towards vehicle electrification and autonomous driving, look set to ensure continued strong growth across all our core segments of Power, MEMS and Wireless. We also see exciting new opportunities too in a sector we call Front End Integration where we can address the additional process steps on the CMOS wafer needed to integrate non traditional "More than Moore" technologies. You can read more on this topic through some of the work we are doing to address challenges in 3D IC and heterogeneous integration here within our SEMICONDUCTOR chapter of LAYERS.**

**A growing business needs a growing team. I am pleased to welcome Admir, Dino, Hossein and Vinoth to BU Semiconductor in their roles as Product Marketing Managers (PMM).**

### Dr. Carlo Tosi
**Head of BU Semiconductor**

Three years after joining Evatec as PMM for Wireless business, Carlo became Head of BU Semiconductor in October 2022. He brings wide academic and industrial experience to his role from his career before joining Evatec. After completing his PhD in thin film semiconductor radiation detectors, he worked in research and technology transfer within thin film photovoltaics before taking on commercial roles including technology management within the Power Semiconductor Industry.

### Admir Asanoski
**PMM – Front End Integration**

After completing his broad apprenticeship in mechanical engineering, Admir went on to gain his Bachelors degree in System Engineering and Microtechnology. Complimenting his thin film know-how in semiconductor applications, his previous work experience in photonics and optoelectronics included responsibility for Application Engineering within BU Optoelectronics at Evatec and gives him a strong focus on delivering the same robust process solutions to customers working in Semiconductor applications.

### Dr. Dino Faralli
**PMM – MEMS**

Dr. Dino Faralli is a physicist gaining his first and postgraduate degrees at the University of Perugia, Italy. He has over 20 years experience working in semiconductor industry. From R&D of new materials to product design, development & testing with successful technology transfer from lab to fab, he is well versed with the device manufacturing environment. His main focus has been on a wide range of MEMS applications and devices including microphones, pressure and magnetic sensors, microfluidics, print-heads, piezoelectric actuators and PMUTs.

### Dr. Hossein Elahipanah
**PMM – Wireless**

Hossein received his PhD in microelectronics from KTH university in Stockholm. He has over 12 years of experience in semiconductor industry ranging from start-ups leading the development and industrialization phase to program management in high volume production for automotive application. He has worked in foundries giving him hands-on experience in fabrication processes and a complete understanding of vertical and lateral process technology, topographical design rule generation, and SPC analysis. He has worked in several technology areas including ultra-high voltage silicon carbide (SiC) and compound semiconductors, low-voltage CMOS and photonic ICs (PICs), RF ICs and ASICs.

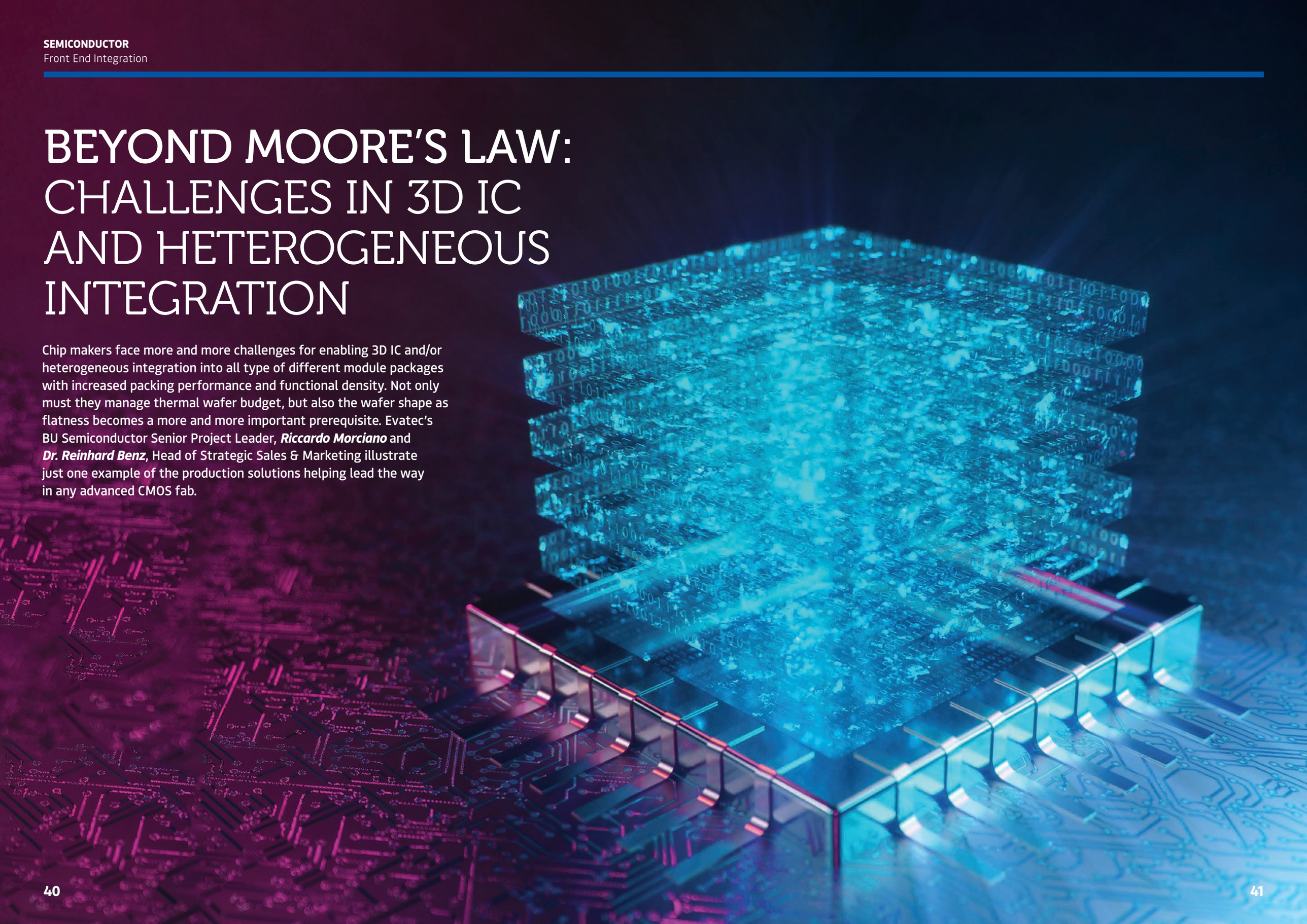
### Dr. Vinoth Sundaramoorthy
**PMM – Power Devices**

Dr. Vinoth Sundaramoorthy has completed his PhD in Semiconductors devices from the University of Nottingham, UK and Executive MBA in General Management from Executive Business School, University of St Gallen.

He has extensive experience in the semiconductor field for over 18 years that includes hand on experience in power semiconductors and related applications development (14 years). In his previous job at ABB Switzerland, he was involved in the product development of various power semiconductor devices and managed several semiconductor related global projects for different business units.

# BEYOND MOORE'S LAW: CHALLENGES IN 3D IC AND HETEROGENEOUS INTEGRATION

Chip makers face more and more challenges for enabling 3D IC and/or heterogeneous integration into all type of different module packages with increased packing performance and functional density. Not only must they manage thermal wafer budget, but also the wafer shape as flatness becomes a more and more important prerequisite. Evatec's BU Semiconductor Senior Project Leader, ***Riccardo Morciano*** and ***Dr. Reinhard Benz***, Head of Strategic Sales & Marketing illustrate just one example of the production solutions helping lead the way in any advanced CMOS fab.



Barriers to protect the CMOS backplane might be needed for embedded or the heterogeneous integration of III-V RF- and/or photonic components. Thin film technology can be an ideal solution to address Front End Integration processes such as stress compensation, heat dissipation, diffusion barrier layers and protection layers and therefore master the complexity of 3D IC and hetrogenous integration challenges. Within the latest hard mask technology there's also a need to lower the thermal budget, moving to lower deposition temperatures with sputtering using new oxides or nitride materials.

## Solutions for advanced 3D NAND

The increasing number of vertically stacked wafers for increased functional and storage density can lead to wafer deformation and a corresponding substrate warpage. One way to overcome these challenges is backside wafer Warpage Correction (WPC) through a dielectric PVD layer prior to subsequent processing steps (see Figure 1).

Using a compressive nitride PVD solution offers tunable stress films at low temperatures. Key specifications for the desired application which must be fulfilled include stress range, layer thickness, substrate temperature and edge roll-off but also chemical properties for potential post-treatments like the and etch removal process.

Warped wafers can be compensated efficiently using films in the thickness range between a few nanometers and micrometers with a correspondingly high bow correction ratio of about 1µm per nm (Figure 2). If a specific film thickness must be maintained, the film stress or warpage correction can be easily adjusted at constant film thickness.

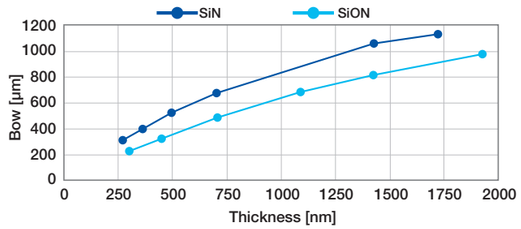



*Figure 2: Warpage-thickness ratio*

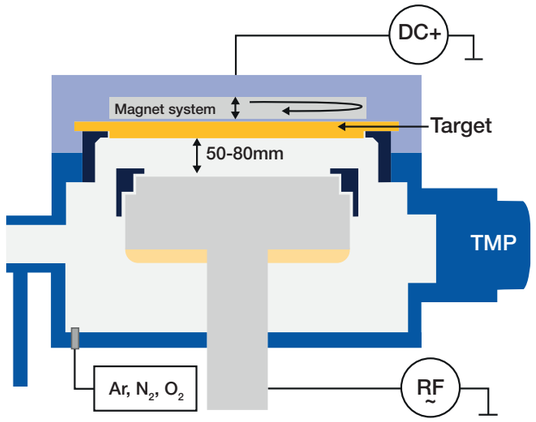



*Figure 3: Sputter module configured for nitride film deposition*

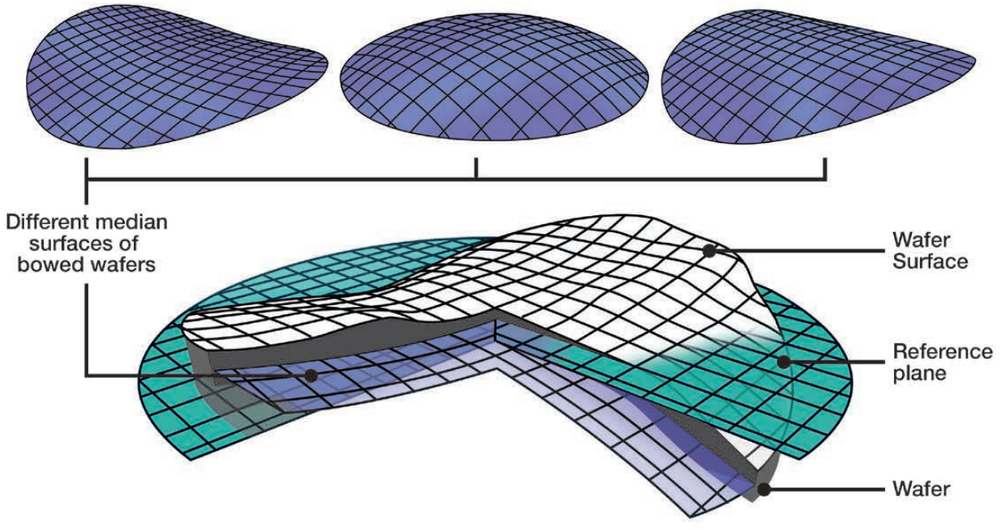



*Figure 1: Conceptualising the transition from warped to flat wafers*

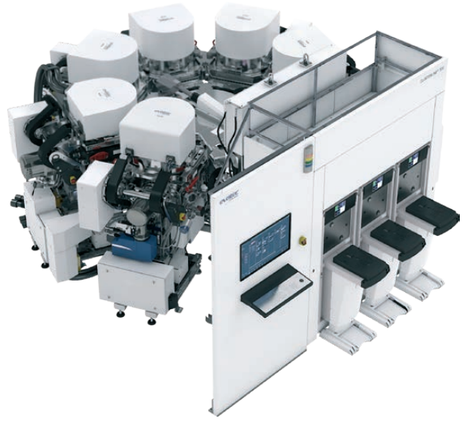


*Figure 4: CLUSTERLINE® 300 with up to 6 PVD (DC) modules*

## CLUSTERLINE® 300 – WPC production solutions are ready

Where the Front End Integration process is part of the BEOL in the CMOS Front End fab, the CLUSTERLINE® 300 platform is available in a dedicated CMOS configuration for improved vacuum, defects and contamination performance.

For the backside Warpage Correction (WPC) application the tool comprises three automatic loadports for 25 wafers (12"), pre-alignment station, flipper and transfer modules included two-arm robot. The sputter modules (with optional shutter) are prepared for nitride film deposition (see Figure 3). A typical tool configuration including 6 DC sputter modules is shown in Figure 4.

Depending on the substrate specification the system can be configured contactless (3mm edge exclusion) and is able to handle warped substrates using dedicated end effectors and shelves. Wafer handling capabilities enable operation with standard Si, thin Si, TAIKO or glass substrates in contamination free <5.0E+10atoms/cm$^2$ environment and the system has production proven parallel processing scheduling capabilities allowing combination of short and long processes.

To find out more about Evatec's latest generation CLUSTERLINE® 300 platform features visit:
**www.evatecnet.com/products/clusterline-family/clusterline-300**

## About the authors

**Riccardo Morciano**
Riccardo has just taken on a new role as Senior Project Leader Development Projects in BU Semiconductor.
His 14 years exeprience in the vacuum and thin film industry at Evatec starting with an apprenticeship, followed by roles incluidng application engineer and project leader stand him in good stead for the challenges ahead.

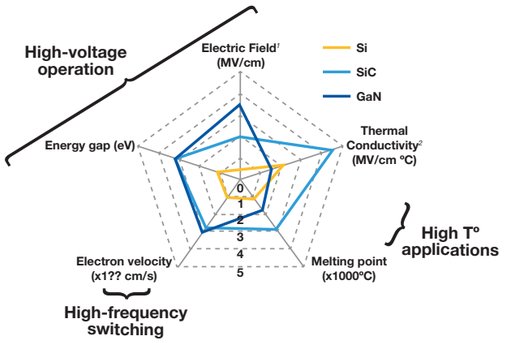
**Dr. Reinhard Benz**
Dr. Reinhard Benz joined Evatec in 2013 as Senior Vice President within the Evatec management team. He is Head of Strategic Sales and Product Marketing. He gained a Doctor of Physics degree (Dr.rer.nat) in Applied Physics of Semiconductors from Eberhard-Karls University in Tübingen, Germany and has more than 30 years experience working in the semiconductor and solar capital equipment industries in Europe, Asia and North America.

# SiC – POWERING AHEAD IN POWER DEVICES

Evatec's Semicondoctor BU process engineering specialists ***Dr. Bernd Heinz*** and ***Gerald Feistritzer*** remind us why Wide Band Gap (WBG) materials like SiC have an exciting role to play in emerging power device applications. They explain how Evatec can leverage its know-how from many years experience on silicon and add new processes like carbon cap layers to help its customers power ahead in SiC technology on CLUSTERLINE®.

## The benefits of Silicon Carbide

In the past decades power semiconductor technology was dominated by Si based devices, but due to its physical properties it seems that Si is reaching its performance limits and that's where wideband materials like SiC could step in. As highlighted in Figure 1, SiC offers three times the band gap of Si, about ten times the dielectric breakdown voltage and significantly better thermal properties like higher melting point and thermal conductivity.




- SiC will remain the preferred choice for high-temperature applications
- GaN could possibly reach high-voltage values, but would require bulk GaN as the substrate - which is not currently possible
- Silicon cannot compete in the high-frequency range

[1] *The electrical field profile can also be controlled by the doping concentration*

[2] *The Tc for GaN is given here for typical GaN-on-Si. It has been demonstrated that the Tc of bulk GaN could reach four W/cm °C*

*Figure 1: Relative merits of Si, SiC and GaN. Ref: Yole Power GaN 2016: Epitaxy, Devices Applications and Technology Trends*

## Evatec – your proven industry partner

Evatec can look back with pride on its long experience in the field of Backside Metallization (BSM) coating on Si technology as a leading supplier of deposition equipment and processes for BSM on thinned wafers where the frontside processing is completed. Our knowledge has helped customers handle these substrates with excellent temperature control even where wafers have significant warpage without harming the frontside structures.

Another typical application in Si technology is trench filling with thick Al(Si,Cu) contacts. The challenges are the sidewall and bottom coverage with Ti and TiN wetting and barrier layers, followed by the subsequent void free filling of the trenches with Al in order to form a planar surface. Some typical backside and frontside processes and the know-how which Evatec offers are shown in Figures 2a, 2b and 2c respectively.

Now we can also leverage all this experience to support customers ramping up their SiC technology.

## The new generation CLUSTERLINE® family delivers even more

Our new CLUSTERLINE® 200 Platform is the right choice for our customers with the capability to handle wafers up to 8 inch supporting a whole array of different power device applications. It builds on the reputation of the previous CLUSTERLINE® 200 II, and extends performance even further with various new improvements including:

- Modular architecture (Configurable with Batch Process Module, Single Process Module (PVD, PVE, PECVD, etc.))
- Upgraded component design offering increased standardization
- Increased process capability
- Enhanced tool uptime combined with reduced cost of maintenance and service
- Upgraded user interface with Evatec XPERIENCE Software
- Standardized and improved component design

We may have made lots of improvements but existing tool customers don't need to wory about compatibility. The new tool uses identical process kits as the previous CLUSTERLINE® 200 II generation (e.g. chucks, shieldings, magnet systems etc.) for high process transparency.

## Protective Carbon Cap Layer processes for SiC

Doping or selective doping is one of the first process steps in SiC power device production. While thermal diffusion doping is a mature technology for other materials, the high melting point of SiC and the low diffusion constant of dopants within the material makes ion implantation the only practical technology for SiC doping. High temperature annealing at ~1600°C is a necessary process step after implantation to ensure lattice damage recovery and the electrical activation of the dopants.

The formation of a high surface roughness due to the desorption of Si atoms at temperatures > 1000°C is known as a critical issue associated with the post implantation annealing process. The most efficient state-of-the-art counter measure to prevent the unwanted roughening is the coverage of the SiC surface with a protective carbon cap layer before annealing. After annealing the remaining carbon can be removed by $O_2$ plasma ashing or oxidation at 700°C – 800°C.

Evatec has developed a dedicated DC sputter process on the CLUSTERLINE® 200 E platform for the cost efficient deposition of carbon layers on 6'' and 8'' SiC substrates. Typical layer results and the source configuration and are shown in Figures 3a and 3b respectively.

To find out more about Evatec process solutions for power device applications on Si, SiC or GaN contact your local Evatec sales and service office.

Learn about Evatec's new CLUSTERLINE® generation.

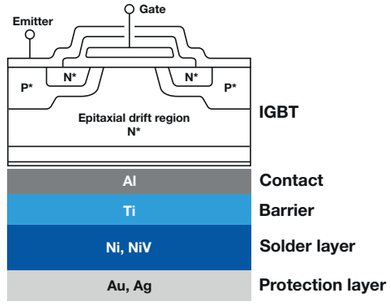



*Figure 2a: Typical backside process*

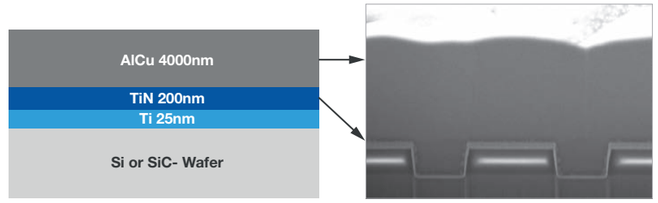


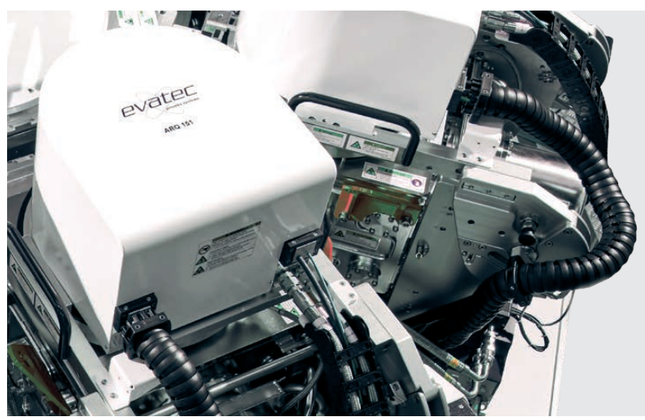

*Figure 2b: Typical backside process*

| Process types | The Evatec Advantage |
|---|---|
| ▪ PVE – Polyimide and metal removal: ICP etch | ▪ Proven processes for pretreatment with Ar etch or $H_2$ capability |
| ▪ PVD – Backside metallization: Al / Ti / NiV / Ni / NiSi / Au / Ag | ▪ Dedicated edge grip hardware to prevent contact with finished frontside<br>▪ Excellent stress control capability |
| ▪ PVD – Frontside barrier and wetting: Ti / TiN | ▪ Different hardware setups available for devices based on planar or trench technology for a proper barrier layer incl. good coverage over the whole trench geometry |
| ▪ PVD – Frontside contact: Al Flow Process | ▪ High Temperature Hardware in place for trench fill and planar surface |

*Figure 2c: Process types and Evatec know-how*

| **Target – Substrate Distance** | 50mm | 125mm |
|---|---|---|
| **Typical film thickness (nm)** | 20 – 400 | |
| **WiW uniformity (%)** | <5% | <15% |
| **Typical deposition rate (nm/s)** | 1.6 | 0.7 |
| **Refractice index** | 2.3 – 2.4 | |
| **Typical film stress (MPa)** | -800 to -400 | |

*Figure 3a: Typical layer specification for carbon capping process on 6" or 8" inch substrates*




- System configuration: Single Process Modules (SPM)
- Vacuum system: Cryo-pump
- 6" or 8" chuck at room temperature
- Shadow mask (full face deposition)
- ARQ 151 DC sputtering 6kW, Ar sputter gas
- Carbon target
- Zoom shield

*Figure 3b: ARQ 151 source for carbon cap deposition on CLUSTERLINE®*

# Power electronics – a booming industry

The power electronics market, for both discrete and modules, is growing very strongly and is expected to be worth an impressive $30.5B by 2027, according to Yole Intelligence, part of Yole Group. It is a fact that ever more electronic systems are required to meet the huge demand from end systems, specifically the need to increase efficiency and reduce $CO_2$ emissions. This includes greener energy generation, more green cars, more charging stations, more energy storage, and more industrial carbon-neutral goals.

All these systems will contribute to the booming market, but the key application driving the market will be electric vehicles (xEV). Governmental initiatives, aided by OEM commitments, will drive the car market to 50% fleet electrification by 2027. Every xEV, whether a PHEV or BEV, will have at least one main inverter, a DC/DC converter, and an onboard charger, which directly translates to power electronic content.

Looking closely at the various component types making up power electronics, three essential items are forecast to take most of the market in the next five years: Silicon MOSFET, IGBTs, and Wide Bandgap devices.

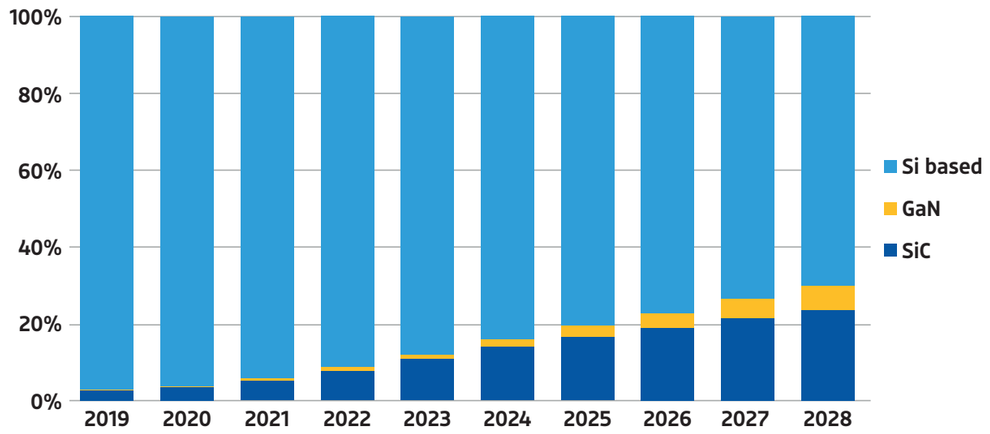
Silicon MOSFET  comprise the largest power market and can be found in consumer electronics, automotive auxiliary systems, and small power industrial applications. The market for Silicon MOSFETs will grow at a 1.3% $CAGR_{2021-2027}$. This smooth increase is related to a big push from industrial and automotive (including xEV) but with a consumer market declining after two exceptional years pushed by COVID lockdowns. GaN will continue grabbing a share of the silicon MOSFET market, mainly for fast chargers for consumer electronics. IGBTs, specifically IGBT modules, are expected to grow with an 8.4% CAGR2021-2027, mainly due to xEVs but also industrial applications and home appliances.

Speaking of xEVs, it's also the main market driver for SiC. Especially with the trend of 800V battery systems, the SiC device market is forecast to reach nearby US$8B by 2028. This is mainly due to the demand for SiC MOSFETs in the main inverter. This, together with energy and industrial applications, such as PV converters and EV charging infrastructure, will drive the SiC market to a $CAGR_{2022-2028}$ of 30%%.

For the Power GaN market, automotive DC-DC converters and OBCs will be part of its next wave of growth after its massive adoption in consumer power supplies. We are seeing more and more collaboration between GaN device players that are accelerating the automotive qualification of their products and the Tier 1s and OEMs that are evaluating automotive GaN solutions. The Power GaN device market for EV applications mainly in OBC and DC/DC segment, is expected to exceed $300M by 2028 with a $CAGR_{2022-2028}$ of 82%.

The entire supply chain is preparing for the increased volumes that this rising demand requires by expanding manufacturing lines. The big semiconductor manufacturers, such as Infineon, onsemi, and Alpha&Omega, have already added 300mm lines to their sites, whereas other significant players like Renesas, Toshiba, and Rohm will open new facilities in the coming 2-3 years. But it is not only device manufacturers that are enlarging capacity: wafer manufacturers (Si and SiC) are also getting ready for capacity increases before 2025. □

**WBG vs Silicon discrete and module power semiconductors**




*Source: Power SiC/GaN Compound Semiconductor Monitor Q1-2023*

**About the authors**

**Ezgi Dogmus, PhD.** is Team Lead Analyst in Compound Semiconductor & Emerging Substrates activity within the Power & Wireless Division at Yole Intelligence, part of Yole Group. Prior to Yole, Ezgi worked as a process development engineer for GaN-based RF and power solutions at IEMN.

**Ana Villamor, Ph.D.** is a Team Lead Analyst for power electronics activities within the Power and Wireless division at Yole Intelligence. Prior to Yole, Ana was involved in a high added-value collaboration within the CNM research center and ON Semiconductor.

# ShanghaiTech University

## Nurturing future talent and collaboration is key to success

ShanghaiTech University is a young, resource-rich university with a modern residential campus in the heart of Shanghai Pudong's Zhangjiang Hi-Tech Park. With an academic focus on STEM research, the university is committed to carrying out top-notch research and nurturing the next generation of innovative scientists, inventors and entrepreneurs. The university seeks cutting-edge solutions to address the challenges that China and the world are facing in the fields of energy, material, environment, human health, and artificial intelligence.

***Professor Wu***

In an interview with LAYERS **Professor Wu** explains more about the work at PMICC, the importance of collaboration, and how thin film technology capability provided by companies like Evatec is helping his own group and others develop world leading piezo thin films and devices.

**Please tell us about work of your department and the field of your research.**

The PMICC center aims to promote the research and applications of novel devices, circuits, and systems. Our mission is to realize high energy-efficient computing for emerging applications from the perspectives of fundamental research core techniques in physical principles, devices, circuits, and systems. The center is exploring technologies ranging from cryogenic electronics, spintronics, optoelectronics, Micro-ElectroMechanical Systems (MEMS), III-V compound semiconductors, electronic design automation, system-on-chip, signal processing, reconfigurable computing, digital circuit design, and custom computing for robotics, smart vehicles, and so on.

At this time we have 18 principal investigators and more than 100 graduate students.. We are also actively participating in several national/CAS key R&D research programs with more than 50,000,000 RMB funding. In addition, under the framework of several research platforms including ShanghaiTech Microelectronics Research Center, ShanghaiTech-UC Berkeley BDMC, and ShanghaiTech Quantum Device Nanofabrication Laboratory (SQDL), we also collaborate with IC companies and universities to push emerging IC research forward.

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上海科技大学 ShanghaiTech University

PMICC 后摩尔器件与集成系统中心 Post-Moore Microelectronics Integrated Circuit Center

### What kind of process and test equipment do you have available?

We are able to offer multiple deposition technologies including sputter, e-beam evaporation, thermal evaporation, PECVD, ALD, LPCVD, etc. plus etch, lithography and a whole range of test equipment measuring film surface profile, thickness,, stress, piezo properties etc. We have a complete 4/6 inch line and can also make development on anything between 2 and 8 inch.

### How do you support the wider academic / industrial community?

We see networking and wide collaboration as key to success. We are located adjacent to some of the leading scientific and research institutions in China. The area also hosts headquarters and R&D centers for many high-tech corporations such as Baidu, Huawei, Tencent, SMIC as well as multi-nationals including Qualcomm, IBM, Pfizer, and Astra-Zeneca.

A number of our faculty graduated from or worked at leading institutions, including MIT, Berkeley, Caltech, UIUC, UCLA, EPFL and others before joining us. We strongly believe that it is through international perspectives as well as value for both innovation and fundamental research that our faculty can impart the highest standards of knowledge and guidance to our students. So an important part of our work is help other groups by providing access to our equipment and know-how.

### How does equipment from Evatec help you in your research?

Our CLUSTERLINE® 200 PVD system provides us with a world-class system and capability for Mo/AlN/AlScN thin film deposition.

We have collaborated with Evatec to achieve high quality AlN/AlScN deposition on Si, $SiO_2$, sapphire, SiC substrates. We have also been able to address the emerging interest in high Sc content AlScN films, especially ratios over 30%, through process development, film quality characterization, piezoelectric acoustic transducer design and testing.

We have already provided sample materials through collaboration with more than 30 universities, institutes or companies in China, Singapore and United States etc.

### What do you see for the future?

The future is all about collaboration - at Shanghaitech Microsystem And noveL transducers Laboratory (SMALL) we are developing chip-scale sensor and actuator systems with novel material and micro/nano-fabrication processes. Specific research areas of interest include Micro-/Nano-Electro-Mechanical System (MEMS/NEMS) design and modeling, novel multiferroic materials, processing and acoustic transducers, MEMS-CMOS IC design as well as their applications in smart hardware, next-generation communication, Internet-Of-Things (IOT) etc. We welcome collaboration with all scientific and engineering groups joining together to explore fascinating micro/nano-technologies. So please do get in touch!

### Nanofabrication Cleanroom


*Elionix ELS F125 Ebeam Lithography System*

*Evatec CLUSTERLINE® 200 Sputtering System*


*Heidelberg Mask Less Aligner MLA150*



## About the work of PMICC

In the past five years, we have published 200+ highly-impact journal papers and 110+ top conference papers, including Science, Science Advances, Nature Materials, Nature Nanotechnology, Nature Communications, Proceedings of the IEEE, Nano Letters, ACS Nano, Optica, ACS Photonics, Electron Device Letters, Applied Physics Letter, JMEMS, Micromachines, IEEE MEMS, TRANSDUCERS, DAC

### Some recent highglights

**1. Journal of Michromechanical Systems**
*High Quality Co-Sputtering AlScN Thin Films for Piezoelectric Lamb-Wave Resonators*
In this article, we have demonstrated optimized AlScN co-sputtering and etching processes in close collaboration with Evatec. High scandium concentrations of the AlScN thin films require more plasma energy during grain growth, which can be achieved by reducing N2 gas flow rate to increase the energy obtained from plasma. However, the N2 flow rate in turn affects the stress. The balance between crystalline quality and stress needs to be considered when selecting the flow rate. In addition, inappropriate energy could lead to Sc accumulation with an increase in the number of abnormal orientation grains. The XRD FWHM of AlScN can be used directly to evaluate the piezoelectric constants. By optimizing the deposition condition, 500 nm Al0.85Sc0.15N thin films with a FWHM of 1.75°, an average stress of –27.5 MPa and a stress range of 107 MPa over 4-inch area are obtained. The dry etching rate of AlScN could be significantly improved by increasing the RF power. An etching rate of 130 nm/min and a profile of over 77° are achieved. Finally, Lamb-wave resonators have been fabricated based on Al0.78Sc0.22N a n d A l0.85Sc0.15N thin films, achieving a quality factor of over 1000, as well as 152% and 80% improvement in electromechanical coupling coefficients, compared to pure AlN thin film devices, respectively. The significant increase in electromechanical coupling coefficients brought by high quality and high Sc-doped AlScN demonstrates the great potential in RF applications.

**https://doi.org/10.1109/JMEMS.2022.3161055**

**2. Jourmnal of Electron Device Letters**
*Low Loss Al0.7Sc0.3N Thin Film Acoustic Delay Lines*
In this work, we have successfully demonstrated the first unidirectional Al0.7Sc0.3N thin film SPUDT ADLs. The fabricated Al0.7Sc0.3N ADL achieves a low IL of 2.27 dB and an FBW of 7.1% at center frequency of 780 MHz. The extracted group velocity of Al0.7Sc0.3N is 8505 m/s. The coupling coefficient boosted by Sc doping enhances the overall performance comparing to the AlN counterparts. Upon further development, AlScN could enable CMOS process compatible piezoelectric acoustic platforms for chip-scale integrated signal processing, sensing, and computing applications.

**https://doi.org/10.1109/LED.2022.3152908**

**3. Journal of Applied Physics Letters**
*Al0.7Sc0.3N butterfly-shaped laterally vibrating resonator with a figure-of-merit (kt2·Qm) over 146*
Our works take advantage of both the fabrication process and device design. Fabrication challenges are addressed with the Al0.7Sc0.3N thin film, especially for piezoelectric thin film sputtering and dry etching. The realized LVRs with butterfly-shaped boundaries agree with the predicted improvement in performance. Compared with the LVRs with flat boundaries, the same LVRs with butterfly-shaped boundaries achieve 40% progress in FoM. Also, a tuning range of 1.8 MHz is achieved for a 304.8 MHz Al0.7Sc0.3N LVR by applying DC voltage in the range of -40 to 40 V. The fabricated LVRs have low-impedance Rm of 7.09 Ω, which is suitable for RF filters. The operating frequency of LVRs can be scaled up to GHz range with advanced lithography tools and high-order lamb wave modes. With the high FoM of 146.2 and high phase velocity of ~7320 m/s, the reported Al0.7Sc0.3N LVRs are promising candidates for use in RF communications in the future.

**Link: https://doi.org/10.1063/5.0090226**

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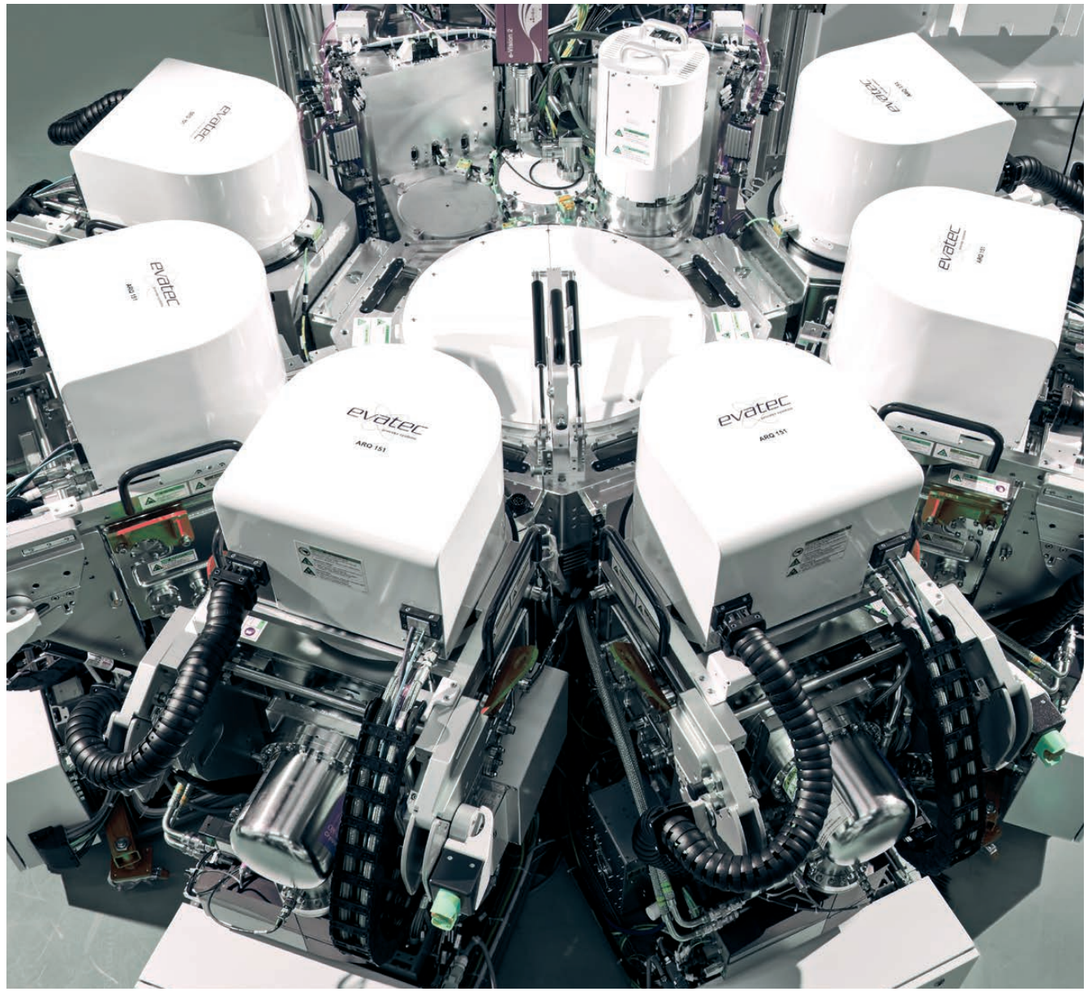
Other companies can access our shared facility through **https://eshare.shanghaitech.edu.cn**

For MEMS/Piezoelectric Transducers fields, please visit **https://small.shanghaitech.edu.cn** or contact Prof. Wu directly.

# MEETING THE CHALLENGES FOR NEW BAW PROCESSES – VERY HOT CHUCK SOLUTIONS

Evatec's Process Engineering Manager ***Martin Kratzer*** (corresponding author) and ***Dr. Xiang Yao*** talk about the technology solutions needed to achieve the deposition processes controlling film crystallinity, stress and thickness uniformity for the thinner films required on 200mm wafers in the RF-BAW filter market.




## The RF Filter market remains buoyant

5G wireless technology is driving huge changes in the telecommunication world with transformation to 5G mobile networks creating enormous opportunities for 5G RF filtering technology. According to statistics from Yole, the overall demand for RF filter units has increased consistently by 8% each year for the last 7 years. In particular, we see a sharp expansion for the RF bulk acoustic wave (BAW) filter market, with ongoing shift from surface acoustic wave (SAW) to bulk acoustic wave due to its superior performance at high frequencies as the BAW filter manufacturing process becomes mature and its cost of production goes down. Currently most of the leading players in the BAW market are American based companies, amongst which Evatec's CLUSTERLINE® system has proven itself to be the system of choice for BAW manufacturing.

## Challenges in BAW technology

The key component of a typical RF BAW filter has a very simple structure. It contains a piezo layer which is sandwiched in-between top and bottom electrode layers. Depending what is underneath the sandwich structure, it is classified as Film Bulk Acoustic Resonator (FBAR), where an air cavity is under the BAW structure, or Solidly Mounted Resonator (SMR), where an acoustic reflector is under the BAW structure. The material of choice is Al1-xScxN, where we utilize its piezoelectric property along the c-axis of its Wurtzite crystal lattice (d33). The choice of electrode material varies, according to considerations for resistivity, acoustic density, and how well the Wurtzite Al1-xScxN lattice grows on top.

The Figure of Merit (FOM) of a BAW resonator is usually defined as the product of the effective electromechanical coupling coefficient keff2 and the quality factor Q. The keff2 is measure of how efficiently the energy is transformed between the mechanical and electrical forms in the resonator and is a consequence of both the piezoelectric coupling coefficient (kt2) of the piezo-layer and the resonator design, while Q is a measure of energy loss in the resonator. In terms of the RF filtering application, keff2 determines the bandwidth of the bandpass filter and Q determines the insertion loss and sharpness of rejection. Development in BAW technology always tends towards higher frequency, broader bandwidth with better power handling performance imposing several challenges for BAW development. Considering the requirements on the Al1-xScxN based piezo-layer, this means a thinner layer structure, as the resonant frequency is inversely proportional to the layer thickness, larger kt2 for wider bandwidth, and better Q factor for loss reduction and power handling. The coupling coefficient kt2 of Al1-xScxN layer is a function of its piezoelectric coefficient d33, which is related to the Sc doping level and the piezo-layer stress, as shown in Figure 2a and 2d. The high kt2 would demand a high level of Sc doping and tensile layer stress. To improve the quality factor, we need to consider the crystallinity of the overall layer structure as well as the electrode design and conductivity.

Nevertheless, the new challenges imposed by the demand for higher frequency, wider bandwidth and better power handling actually put constraints on each other. To utilize the piezoelectric coefficient along the c-axis (d33) of the Al1-xScxN Wurtzite lattice for filtering, a preferential grain orientation, the c-axis <0002> perpendicular to the film surface, is required for the piezo-layer. A measure of how well the Al1-xScxN grains are aligned is the rocking curve (RC) of the <0002> peak in the X-ray diffractometry. Generally speaking, a narrower RC FWHM (full width at half maximum) results in a higher kt2 and Q factor. However, reducing the film thickness usually leads to broader RC FWHM (Figure 2b). Additionally, thinner films tend to show more compressive stress (Figure 2c) due to the lowered wafer temperature during deposition. This again deteriorates the performance of thin films for high frequency

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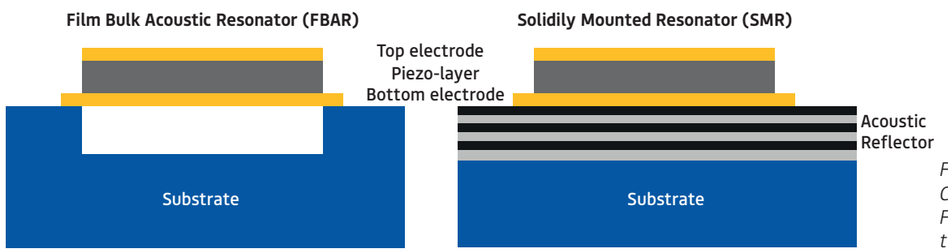


*Figure 1: Comparison of FBAR and SMR technologies*

applications. Sc doping in AlN would enhance the piezoelectric coefficient of the material, thus increasing the $k_t^2$ of the piezo-layer in principle. However, when the $Al_{1-x}Sc_xN$ films are doped with high Sc concentrations, the films are usually more compressive in stress and we also face difficulties to align the grains with c-axis orientation out-of-plane. Especially when Sc doping level is high, abnormally orientated grains (AOGs) form through the whole film thickness and roughen the film surface. These are grains with unwanted orientations which worsen the $k_t^2$ and Q factor of the film. These all cancel the benefit of high Sc doping. On the other hand, if we want to increase the film stress for better $k_t^2$, we usually end up with more AOGs. To sum up, when we deposit $Al_{1-x}Sc_xN$ with low thickness and high Sc concentration, we face problems with compressive stress, broader RC FWHM, and more AOGs. So, is there a way that would allow us to overcome those unwanted effects? A very simple solution is to increase the deposition temperature, which would improve both the film stress and crystallinity, and that brings us to the focus of this article.

For high frequency filtering applications, very thin layer of highly Sc-doped $Al_{1-x}Sc_xN$ films are usually chosen as the piezo-layer. This puts much tighter requirements on the film thickness and stress uniformity. The correlation between $k_t^2$ and film stress depends on the Sc doping level: the higher the Sc doping, the stronger the correlation. As shown in Figure 2d, for 30% Sc doped $Al_{1-x}Sc_xN$ film, the $k_t^2$ changes by 1% per 100 MPa, which is huge in terms of band width at high frequencies for the filter device. Therefore, much narrower stress variation across wafer is needed to guarantee the production yield. Evatec has proven expertise in this process optimization and has already demonstrated an optimized sputter source and process kit.

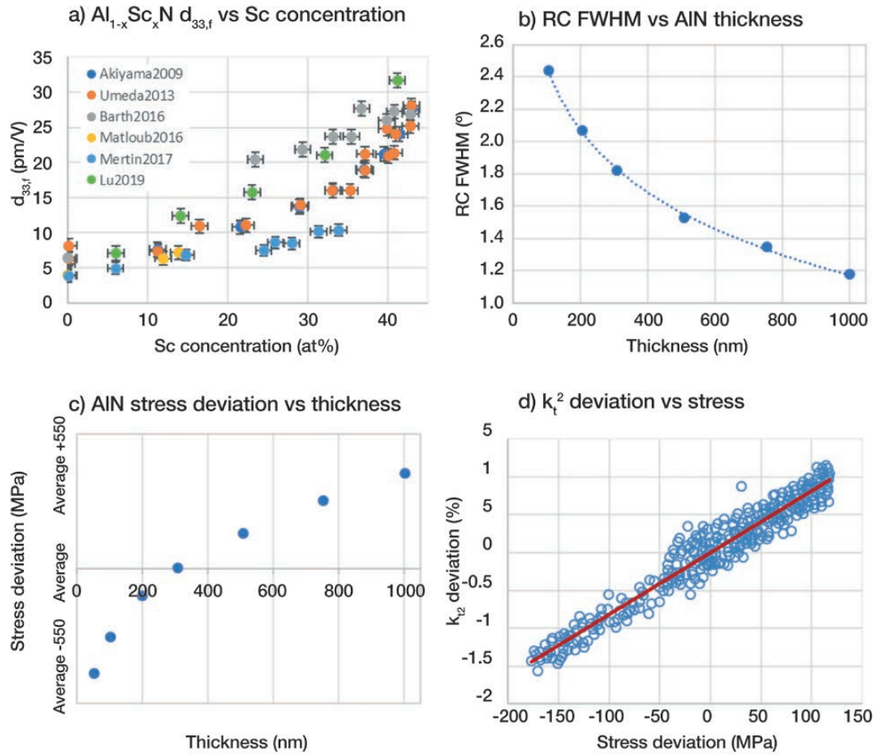


*Figure 2: a) $d_{33,f}$ of $Al_{1-x}Sc_xN$ vs Sc concentration, data are collected from Akiyama et al. [1], Umeda et al. [2], Barth et al. [3], Matloub et al. [4], Mertin et al. [5] and Lu [6]. Error bars indicate only the errors from data collection, not the original data error; b) RC FWHM vs AlN thickness; c) AlN stress deviation vs thickness; d) $k_t^2$ deviation of $Al_{0.7}Sc_{0.3}N$ film vs stress.*

## Managing stress and thickness uniformity in production

Currently at Evatec, we adopt two approaches to meet the increasing demand for stress and thickness uniformity. The first approach is based on the already optimized CLUSTERLINE® 200 module with an upgrade of sputter source from ARQ151 DC to ARQ 151 RFDC. We call this upgrade 'High Performance Package' (HPP) where we switch from DC pulsed sputtering to DC+RF sputtering. This offers us additional knobs for very fine optimization of $Al_{1-x}Sc_xN$ film stress. The HPP package offers dramatic improvement in terms of stress range. We can successfully bring down the stress range below 100 MPa for $Al_{1-x}Sc_xN$ film. One example is illustrated for a 20% Sc doped $Al_{1-x}Sc_xN$ film in Figure 3a. In the second approach illustrated in Figure 3b, we show how we can make still further improvements by modifying the DC sputter source usually used for a CLUSTERLINE® 300 module and installing it on a CLUSTERLINE® 200 module with an optimized process kit. Benefited from the large target size, we can achieve excellent thickness uniformity and stress range. The example in Figure 3b shows excellent uniformities below 0.25% and stress range of 100 MPa for 1um AlN film. It has to be noted that all the measurements in Figure 3 were done with 5 mm edge exclusion. The FSM stress measurements were done with 4 lines across the wafer center.

### Very Hot Chuck Solutions

The modular design of CLUSTERLINE® platforms offers the flexibility to combine different sputter sources, process kits and chuck types to target the best film performance. With this advantage, we can easily incorporate Very Hot Chuck (VHC) solutions into the

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**a) ARQ 151 RFDC source (HPP package)**
With ESC chuck type

| Material | | $Al_{0.8}Sc_{0.2}N$ |
|---|---|---|
| Thickness | | 498.9 nm |
| Thick. 1sigma | | 0.51% |
| Stress | | 16 MPa |
| Stress range | | 82 MPa |
| RC | 0 mm | 1.52° |
| | 60 mm | 1.95° |
| | 90 mm | 1.71° |

**b) ARQ XT source**
With ESC chuck type

| Material | | AlN |
|---|---|---|
| Thickness | | 999.6 nm |
| Thick. 1sigma | | 0.23% |
| Stress | | 20 MPa |
| Stress range | | 100 MPa |
| RC | 0 mm | 1.18° |
| | 60 mm | 1.15° |
| | 90 mm | 1.13° |

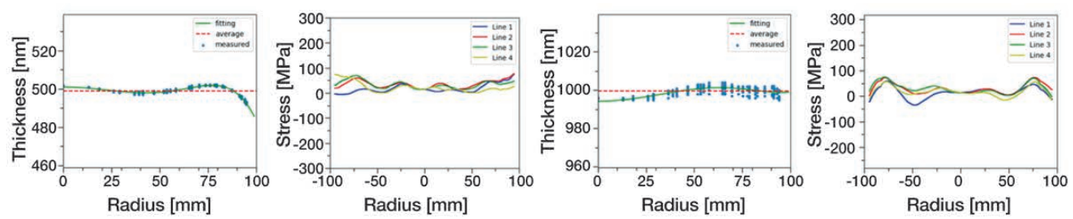


*Figure 3: a) Benchmark film performance for $Al_{0.8}Sc_{0.2}N$ film deposition with ARQ151 HPP package; b) Benchmark film performance for AlN film deposition with ARQ-XT source. It has to be noted that the edge exclusion is 5mm for all measurements. FSM measurements were done with 4 lines across the wafer center.*

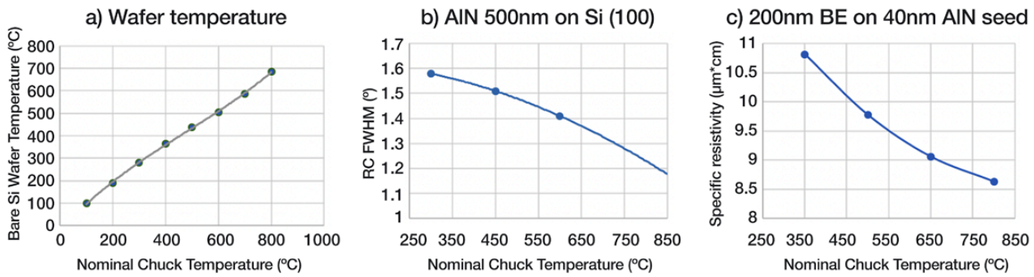


*Figure 4: a) wafer temperature measured by thermal couple array wafer at different nominal chuck temperatures of the VHC; b) RC FWHM of AlN 500 nm film at different nominal chuck temperatures of the VHC; c) specific resistivity of a 200 nm bottom electrode (BE) layer at different nominal chuck temperatures of the VHC.*

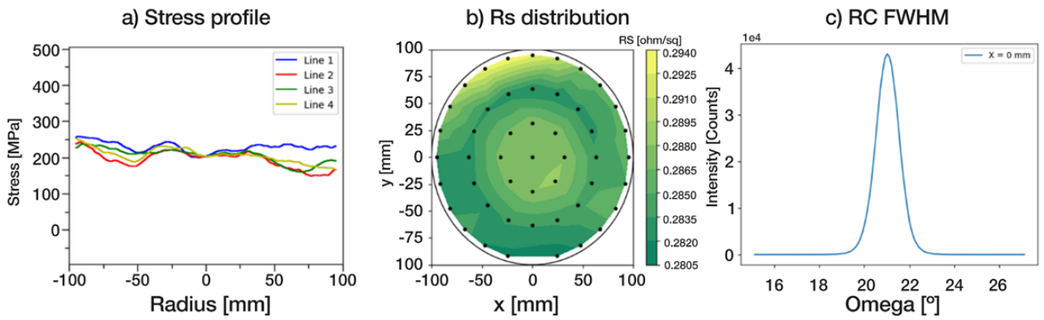


*Figure 5: Film performance of one type of bottom electrode (BE) deposited at 800°C by the VHC. a) stress profile across wafer of the bottom electrode with seed layer; b) Rs distribution across wafer; c) RC FWHM at the wafer center.*

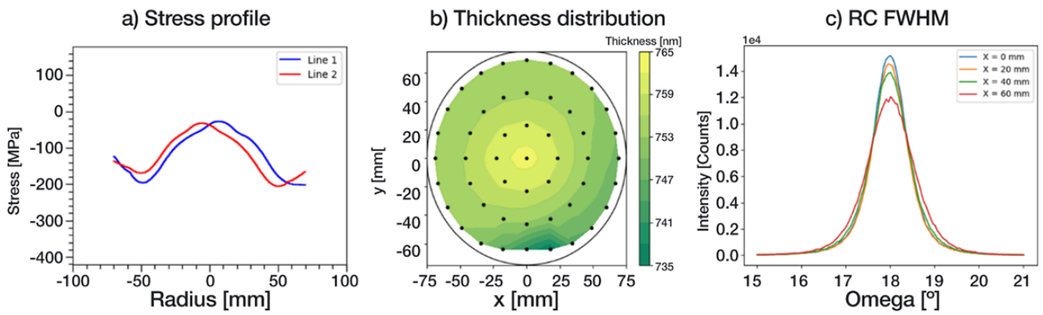


*Figure 6: Preliminary results of AlN deposition by VHC at 600°C. a) stress profile across wafer; b) thickness distribution across wafer; c) AlN (0002) RC FWHM at different radial positions.*



sputter module with the optimized sputter source and process kits discussed above. The VHC has the capability for temperatures to 800°C. Figure 4a shows wafer temperature measured by thermal couple varying chuck temperatures. With chuck temperature heated up to 800°C, the wafer temperature reaches 700°C offering us a much wider range of temperature for deposition. Preliminary results already show the benefit of high temperature deposition. For example, for deposition of AlN on a Si wafer (Figure 4b), we see decreasing RC FWHM with increasing chuck temperature. Similarly, for bottom electrode (BE) layer deposition, the specific resistivity decreases with increasing chuck temperature (Figure 4c). And in the specific example shown here, we could show that resistivity of this type of electrode improved by more than 20% when we increased the chuck temperature from 350°C to 800°C.

Figure 5 shows one excellent example for the bottom electrode deposition with the 8'' VHC. What we see here is outstanding stress range (<110MPa), excellent sheet resistance (Rs) uniformity (< 0.8%) with very low specific resistivity (only 8.28 uOhm*cm) and impressive RC FWHM for such thin layer thickness (1.2°). This film performance exceeds all the bottom electrode specs developed with the original ESC chuck at 350°C.

The VHC deposition of $Al_{1-x}Sc_xN$ is in the development phase at the moment, but it already shows promising results. In the example in Figure 6 we achieve the rocking curve FWHM below 1° with a chuck temperature of 600°C. Despite using mechanical wafer clamping for the very hot chuck tests here, we still see very similar stress and thickness profiles for the deposited film, suggesting that we can in principle preserve the stress and thickness uniformity developed with ESC chuck.

Last but not the least, the VHC also has the advantage of active chuck bias control with RF power applied to the chuck. The process tuning parameters remain the same as the original chuck type.

## The way ahead

VHC looks set to provide a solution meeting the new challenges for further development of BAW technology. With heating capability to 800°C, we can improve the film crystallinity dramatically. In the meantime, we are also able to retain the film stress and thickness uniformity performance with the existing process kit and source. Film stress can still be controlled by RF bias on the chuck. This is a critical feature of the VHC as high temperature deposition on Si wafers usually leads to a very tensile thermal stress. The VHC has the capability to compensate the thermal stress with RF bias. Mechanical clamping is used for the current setup with backgas underneath the wafer for enhanced thermal coupling between the wafer and the chuck. To meet the demand for full-face deposition, we are developing a clampless version of VHC.

Overall, the flexibility and modular design of the CLUSTERLINE® platform places it in a strong position to cater to the changing needs of RF filter manufacturers and meet the challenges of future technology development. ◻

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# OPTOELECTRONICS
# NEWS



> From my perspective, Optoelectronics is the most exciting market. As we look to the future everything will be smaller, lighter, and more energy efficient. Today's science-fiction will become tomorrow's reality.

**Jakob Bollhalder**
Head of BU Optoelectronics

# WELCOME TO THE WORLD OF ITO

From conventional LED to Mini & Micro LED or OLED on CMOS, the nature of ITO films and their interface with others plays a huge role in determining end device performance. Evatec specialists ***Hanspeter Friedli*** and ***Aikaterini Raftopoulou*** talk us through some of the film ITO properties which can be influenced through deposition conditions and how important it is to work in partnership with device manufacturers for developing an understanding of how each might be optimised for their own particular application.

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## What ITO film properties can we vary?

Device manufacturers are continuously seeking to improve their overall device performance, typically through Forward Voltage (Vf) values which should be low and light outputs (LOP) which should be as high as possible. Here are some of the typical film properties we are have been asked to tailor for customers in the search for optimum ITO films and the results we have achieved so far.


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# Resistance

One of the most typical characteristics specified by customers is sheet or specific resistance which can be varied hugely according to the deposition process conditions chosen. These include RF/ DC ratio, oxygen flow and if deposition takes place cold or hot. The range of typical values we are often asked for is illustrated in the table below.

## Achievements

| Typical specific resistance values (after anneal): | | |
|---|---|---|
| for cold ITO | min: ~160μΩcm | up to max: ~400μΩcm or higher |
| for hot ITO | min: ~100μΩcm | up to max: ~400μΩcm or higher |

Sheet resistance is also dependent on grain size, with typical results showing strong correlation for films with grain size less than 1 micron (see Figure 1).

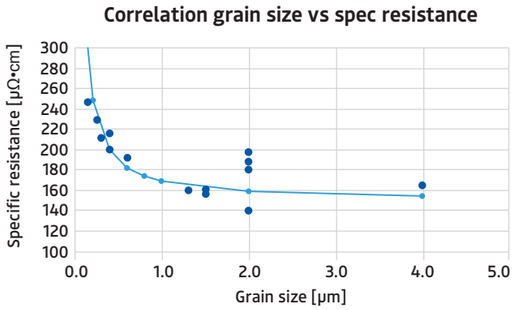



*Figure 1: Specific resistance versus ITO film grain size*

## Achievements

Dependence resistance vs LOP

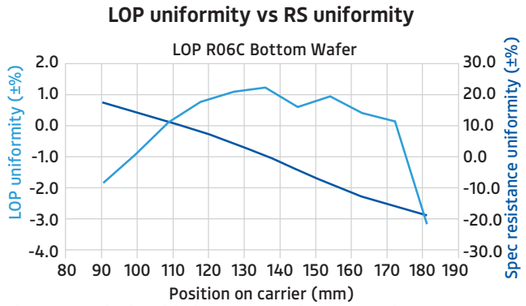



*Figure 2: Relationship between resistance and LOP*

When talking about ITO its important to remember that sheet resistance values refer to annealed films. Whenever we talk about specifications for sheet resistance we work together with customers to help them develop the widest possible process window by understanding their process flow – for example, whether anneal is done at the time of deposition of later on downsteam in their process.

Whilst ITO film resistance values may have an influence over other device performance criteria, we do know however from working together with customers that sheet resistance is not a tool we can use to modify Light Output Performance (LOP). In Figure 2, we can see LOP values plotted at different positions on a 200mm wafer and how film resistance values vary. There seems to be no correlation.

"We have more than 10 years experience in 'low damage' processes for ITO depostion"
**Aikaterini Raftopoulou**



# Transmission

In general, we are looking for high transmission / low absorption films after anneal. Transmission values achievable vary considerably with both film thickness and the deposition conditions used. There are important dependencies between thickness uniformities and transmission. Some typical achievements are shown in the table below.

Every customer has different requirements, so it can be a trade off between what transmission values and thickness uniformity are acceptable. Again we like to work together with customers always thinking about the end properties required for annealed films. Using other variables like RF/ DC ratio or gas flows also helps us develop the widest possible process window. The transmission performance of some typical films is shown in figures 3a and 3b.

## Achievements

| Typical transmission values after anneal are:<br>measured @ 450nm |
|---|
| for ~1100Å:<br>> 98.5% with perfect thickness uniformity (< ± 0.6% on 6 inch) |
| for ~200Å:<br>max ~98% with worse thickness uniformity (< ± 1.5% on 6 inch)<br>max ~96.5% with better thickness uniformity (< ± 0.8% on 6 inch) |

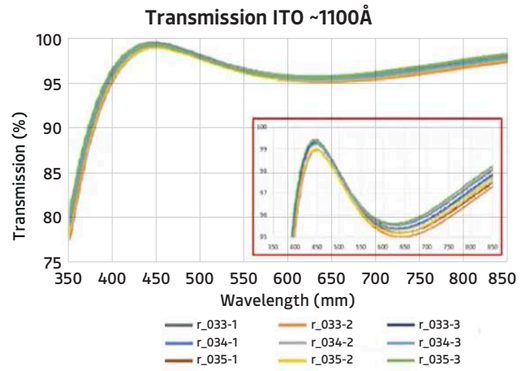



*Figure 3a: Typical transmission performance for a thick ITO film*


*Figure 3b: Typical transmission perfromance for a thin ITO*

# Film Uniformity

Over the last years we have seen a trend to customers requiring both thin films in the range (150Å to 300Å) and thick films (1000Å to 3000Å), with very high uniformities in both cases. As you can imagine, measuring uniformities accurately for very thin films is challenging but you see some typical results that we have achieved on our high throughput CLUSTERLINE® 200 BPM tool where the use of rotating chucks is very helpful to achieve such good uniformities in figure 4. Optimising process conditions for film uniformity will certainly influence device performance properties like Vf or LOP but not always in a direction that we might first expect so we certainly need to optimise other process variables too to achieve the results our customers are looking for.

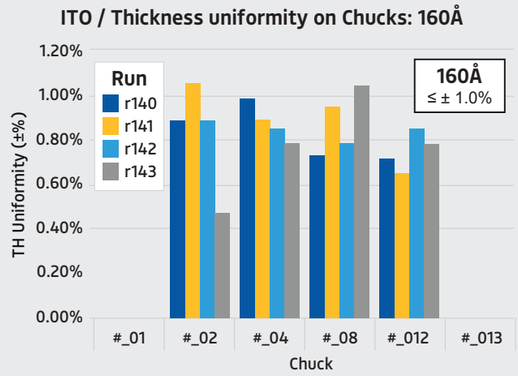



*Figure 4a: Thickness uniforimity for a thin film*

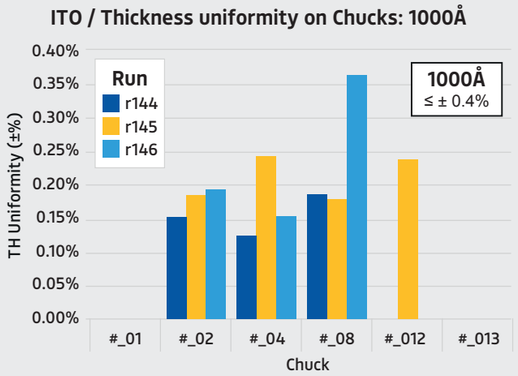



*Figure 4b: Thickness uniforimity for a thick film*

# Film Roughness

Typically our customers call for low roughness values. The micrographs in figure 5 show how changing deposition conditions like RF/ DC ratio for cold deposition of 300Å films has a large impact on grain size but almost no influence on Ra value which remains in the range 0.1 to 0.2nm.

For hot deposition however, we see its generally possible to deliver much higher variation of Ra values in the range 0.5 to 2nm. Varying conditions for hot deposition processes has been as an effective tool to achieve the specific film roughnesses requested by the some customers, but understanding the influence of film roughness values like Ra on device performance is certainly an area we are seeking to understand in more detail going forwards.

Depending on anneal conditions we can observe specific film features like needles occurring (see Figure 6). While such changes might not be picked up in Ra measurements, they would however have a strong influence on any measured Rz values, so it is also important to distinguish between different roughness parameters too.

While these can be controlled according to our choice of exact anneal conditions such as temperature and process gas this will in turn have an influence on device performance characteristics like Vf/ LOP.

**Achievements**

LOWEST roughness films are typically made as COLD deposition

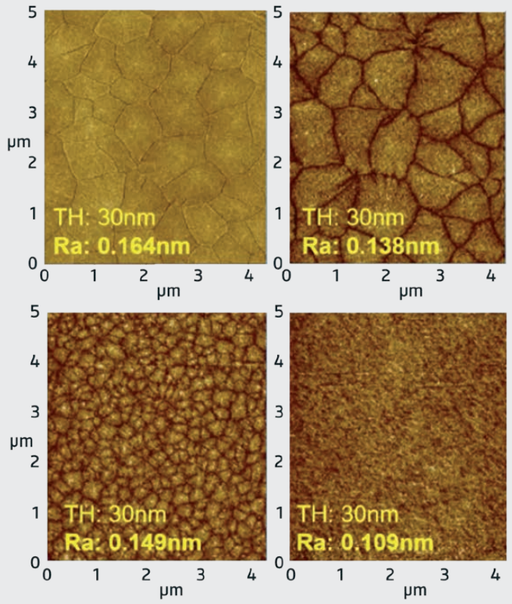



*Figure 5: Films with very differing grain sizes can have very similar Ra values (note scan aresa 4x5µm)*

"Even after more than 20 years of working on ITO there is still so much to learn... and thats what makes it so exciting"
**Hanspeter Friedli**

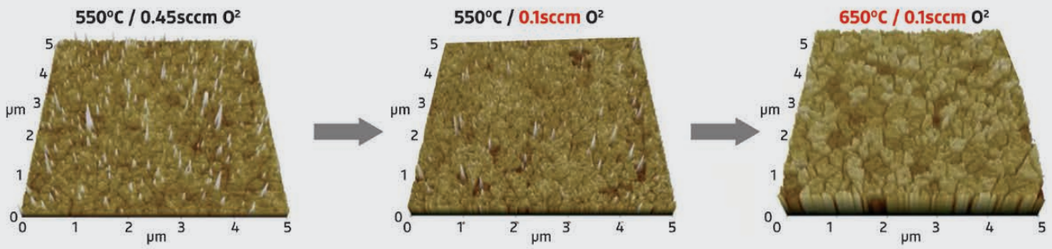
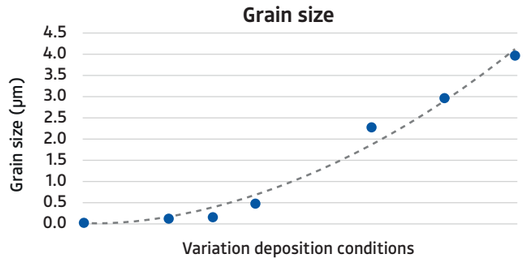


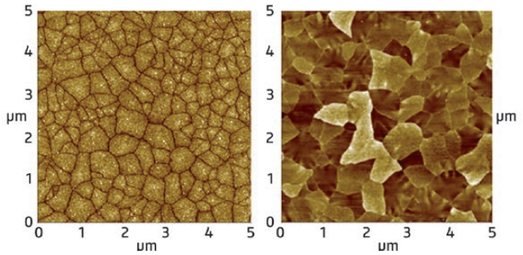

*Figure 6: Influence of annealing conditions of film morphology.*

# Grain Size

Cold deposition processes tend to produce more rounded grains relative to hot deposition, but in both cases we have effective tools to control grain sizes from small to large.

Figure 7 shows how we can use our know-how to achieve film grain sizes that are optimal for each customer device.




**Typical grain size for COLD deposition**

**Typical grain size for HOT deposition**

*Figure 7: Effective management of grain size*

# Step coverage

For certain LED device designs with high aspect ratio "pilar" structures we also see a demand for achieving good step coverage on the side wall. Controlling a number of parameters including deposition geometries and process pressures has certainly given us results in an acceptable range so far but its still early days in our investigations.

## How do we find the ultimate conditions?

It's complex... and its only by working closely together in detailed studies with device manufacturers that we can help them improve their device LOP and Vf values. Such studies may help us understand identify general trends for the influence of individual film parameters but one thing is clear... there is no perfect "one solution fits all" process. Every customer and every device architecture is different with different GaN properties. The optimum will also be different for bulk layer or contact layer processes, and how each customers' anneal processes differ, – e.g. what temperatures?, what gas flows?

Having said all that, through all the experience we have gained in the last 10 years its clear that we have a good handle on practical processes that work in production. We have a pretty good understanding of the process limits we can work within to maintain acceptable Vf values and we also have Best Known Methods (BKM) that are a great starting point.

Fine tuning these for customers is just part of our daily business

## So what else are we working on?

**Contact resistance of ITO films to EPI layer**

It's a tricky parameter as it's not easy to measure but its certainly important.

In house computer simulations have already shown that contact resistance is a dominant factor influencing Vf and LOP. The cooperation with customers is highly important to measure the contact resistance on specific customer GaN. This close cooperation will ultimately lead to higher LOP and lower Vf.

# insights
Optoelectronics

***Jakob Bollhalder***, Head of BU Optoelectronics answers questions on the role of the industry going forward, the challenges it faces and how Evatec can contribute.

**Q: What attracts you to the role driving Evatec's activities in the optoelectronics market?**

The optoelectronics market is definitely one of the most exciting markets I have ever worked in. Significant changes in device technology are coming at exactly the same time as customers change from partly manually operated production to semiconductor type operations.

Back in 2018 the industry was just in between two investment cycles. Regular LED technology was mature, mainly cost driven and did not see much investment, while emerging technologies, such as micro LED had not yet taken off. We took our time and kept in close contact with our customers getting to understand their technology and needs. In the meantime Evatec developed the all new CLUSTERLINE® E platform addressing future market needs not only for optoelectronics but also other Evatec core markets like semiconductor. All in all it has been a very productive time and now we are ready to support the future growth of our industry. It's great to be working in markets which are changing so quickly and ones which look set to enjoy strong, long-term growth because they include not only automotive or general lighting, but many other applications like TV, wearables, horticulture, UV-C for sterilization and so on.

**Q: Tell us about the particular market segments that BU Optoelectronics is addressing?**

I like to think that we address all market segments where light is generated, from discrete LEDs (including mini and micro LED with transfer), and LED displays with monolithic integration to Laser Diodes (such as Edge emitting lasers and VCSEL). However, we are always keen to investigate new opportunities together with our customers and external research institutes.

**Q: What are the major trends in these markets that are driving Evatec's activities right now?**

The major trends are currently consumer products, such as new generation Displays with a highly resolved backlight consisting of mini LED as competition to the OLED products which have been in the market for quite some time. In addition, the need for micro LEDs which show even higher resolutions is about to pick-up ending up within the first high-end TVs and wearables as a mass market products in the consumer market most likely in 2024.

We also see different geographical approaches to the way miniaturization of devices is taking place. While Asia, mainly China, is working with existing wafer sizes and reducing device sizes step by step, Europe and North-American activities are already focused on bigger wafer sizes, semiconductor type operations and a much higher device density on the wafer.

**Q: What do you see as the biggest challenges faced in these markets over the next 5 years and how can Evatec contribute?**

The biggest challenge, at least for Micro LED, in the next 5 years will be to get the wafer and production yield up to drive down costs. We also see competing technologies in the market which will also require different coating technologies. The Laser market including LIDAR applications is not so easy to predict. While customers are currently working on driving up their yield, the next years will see further applications, especially in the automotive and datacomms environment, which should also drive further investments. The challenge there is to understand when this will happen. Working in close partnership with our customers supporting both new technology and process developments remains the best way to be ready whichever direction the market heads!

**Q: What have been the highlights for BU Optoelectronics over the last 12 months and what can we expect from you in the rest of 2023 and beyond?**

It's always a highlight to work so closely with so many of our customers supporting roll out of their technology roadmaps and investment in new generation coating systems. We have also been qualified by major customers for production of mini and micro LED devices. Some of them can already be purchased.

**Q: Is there any overlap with other BUs at Evatec and how do you collaborate?**

Yes, definitely. This is another exciting part of my work at Evatec, looking over my shoulder to my collegues to see similar application and challenges, like particle reduction, smaller devices, improved process control etc. Besides this, many of our customers have multiple links with us addressing their different products and markets or contact with us to support their future business development. ◻

# MiniLED & MicroLED

## Two different technologies and applications transforming the display world

The term MiniLED and MicroLED are often used interchangeably but they differ significantly. LED chips below 50 µm are often considered MicroLED, but some large players extend this definition to sizes 100 µm and above. Size alone is not a determinant. Manufacturing technologies and applications must also be considered to properly distinguish micro and MiniLEDs (figure 1).

MiniLED are used to create full-array local dimming LCD backlights with a high number of individually controllable zones which boost contrast allowing perfect black, close to that of OLEDs and very high peak brightness. Those backlights can be seen as low resolution, monochromatic displays placed behind the LCD matrix (Figure 2). The drawback is a "halo" effect that can surround bright objects when displayed on a dark background. This stems from the fact that the number of backlight zones can not match that of the objects to be displayed.

MiniLED backlights are rapidly increasing their presence in high end TVs, monitors, or in Apple's 12.9" iPad pro. For other consumer applications though, OLED remains a formidable competitor with cost, performance and availability improving on a regular basis.

For this application, LED die sizes are typically 200 to 500 µm, so nothing really "mini" about it. Those LED however have unique requirements. The optical design of the backlight is critical to ensure homogeneous brightness across its entire area while, at the same time, limiting optical crosstalk from one zone to another. The LED chips must therefore deliver a broad emission pattern. This is achieved by adding complex dielectric filters on one or both sides. Some of those filters require up to 26 pairs of thin-film dielectric materials.

Another application for MiniLED is for Direct View LED Displays (DVLDs), the large LED displays seen in stadium, shopping malls, concerts etc. Here, each red, green, and blue LEDs sub-pixels is constituted by an individual LED chip. With increasing demand for high resolution, small pitch displays, smaller chip size is paramount for both cost and performance. Sizes of 75x125 µm are already used and the industry is developing 50x100 µm. This poses some challenges, such as electromigration of metals between the pads that could short the LED after a few hundred hours of operation. However, pending some adjustment, MiniLED can be manufactured in existing LED fabs.

This is a different story for MicroLEDs. Just like DVLDs, MicroLED displays are self-emissive, but are targeting consumer applications such as TVs, wearable etc. (see figure 3). To be competitive with OLED in term of cost, chip sizes below 10 µm for TV or even 3 µm for smartphones are needed. Augmented Reality will even require LEDs below 1 µm. MicroLED will require dedicated fabs with better clean-rooms, stepper lithography, and equipment such as Atomic Layer Deposition (ALD), laser lift off etc.

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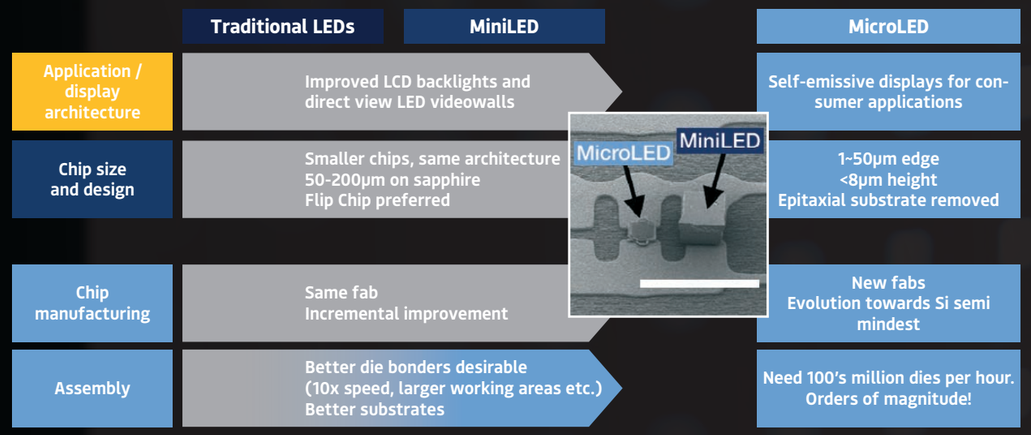


*Figure 1: MiniLED vs. MicroLED. Source: MiniLED report, Yole Intelligence, 2022*

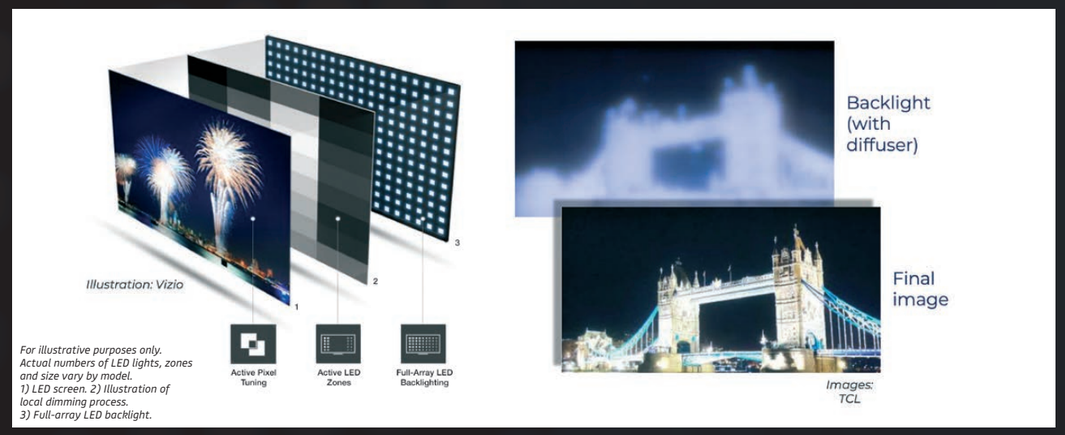


*Figure 2: Full Array Local Dimming LCD backlights. Source: MiniLED report, Yole Intelligence, 2022*

To deliver very small dies at a high yield (>4N) and low cost, there is a need for a paradigm shift toward a semiconductor-like manufacturing mindset, with high-efficiency, automation, end-to-end defect prevention and yield management strategies. Osram recently announced an 800M€ investment to build a 200mm MicroLED fab aimed at serving Apple's needs for its MicroLED Smartwatch. The manufacturing ramp initially scheduled for 2024 is already being pushed back to 2025, illustrating the complexity of the technology and setting the supply chain, including for other critical manufacturing steps such as mass transfer or backplane integration. Smartphones could be next after 2027. In the shorter term, MicroLED have potential for automotive and TVs. For the latter though, another 20x or so cost reduction is required: Samsung's 89" MicroLED TV, which was due to be released by the end of 2022 after multiple delays still costs close to $100,000.

While MiniLED are already successful in both consumer and industrial applications (see figure 4), the future of MicroLED is uncertain with many challenges still be solved to bring costs at levels competitive with OLEDs. For TVs. Smartphones, automotive and basically any large display with low pixel density, disruptive mass transfer technologies that can assemble 100's of millions of LEDs per hour are required. For near eye microdisplays used in augmented reality applications and some automotive Head Up Displays (HUDs), the preferred approach is monolithic integration, where the full high-density MicroLED array is directly bonded onto the Si-CMOS wafer containing the circuits to drive each pixel (see Figure 5).

Despite all the remaining challenges, MicroLED has entered a virtuous development cycle (see Figure 6) with rapidly improving technology, availability of off the shelve equipment, and many large companies investing massively in both R&D and manufacturing infrastructure. ◻

## About the author

**Dr. Eric Virey** is a senior market and technology analyst at Yole Intelligence and is a daily contributor to the development of LED, OLED, and display activities at Yole Group. Previously, Eric has held various R&D, engineering, manufacturing and business development positions with the Fortune 500 Company Saint-Gobain. Dr. Eric Virey holds a PhD in Optoelectronics from the National Polytechnic Institute of Grenoble.

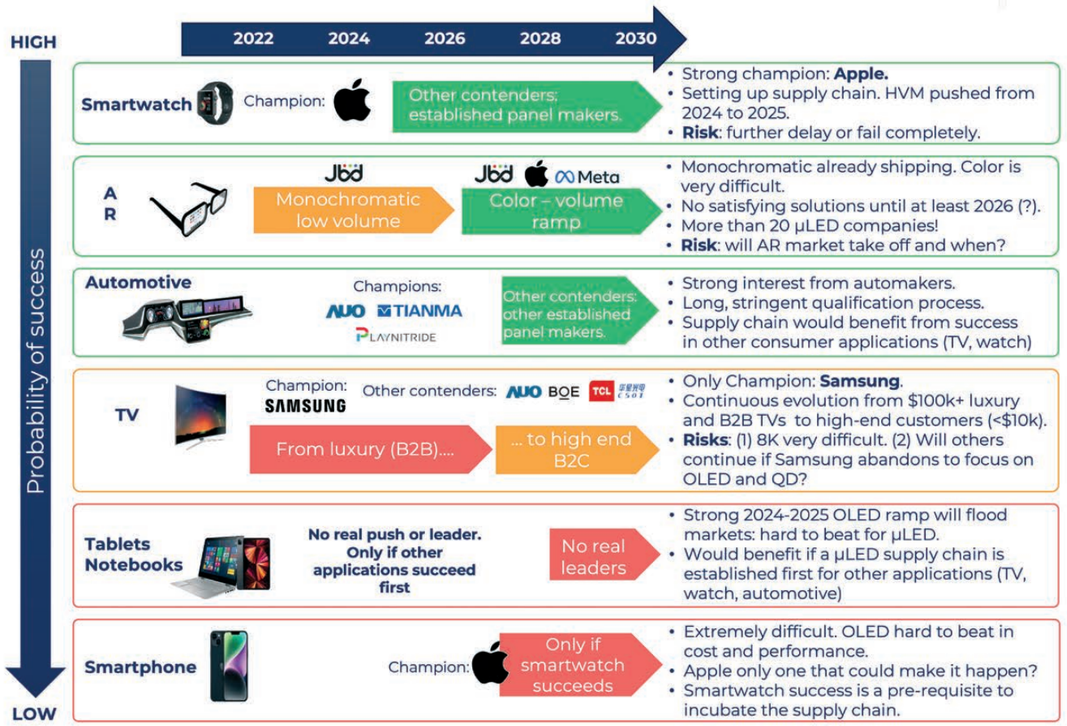


*Figure 3: MicroLED application roadmap. Source: MicroLED report, Yole Intelligence, 2022.*

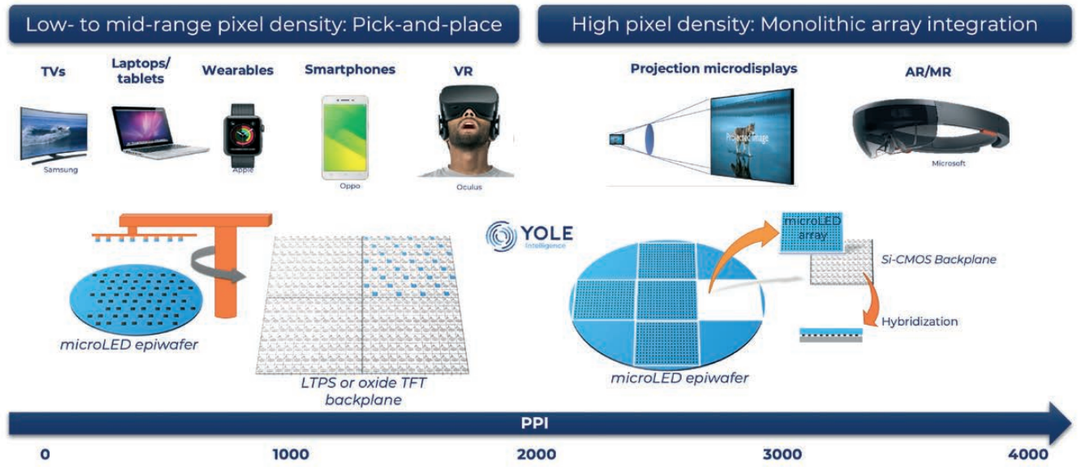


*Figure 5: MicroLED are promising microdisplay technologies for AR/MR & HUD applications*
*Source: MicroLED report, Yole Intelligence, 2022*

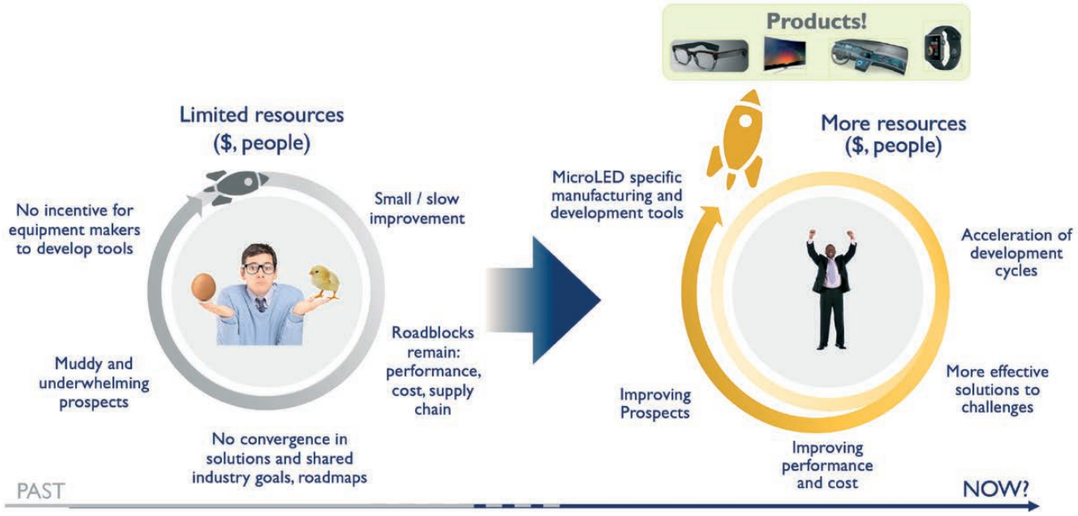


*Figure 6: MicroLED Virtuous Development cycle. Source: MicroLED report, Yole Intelligence, 2022*

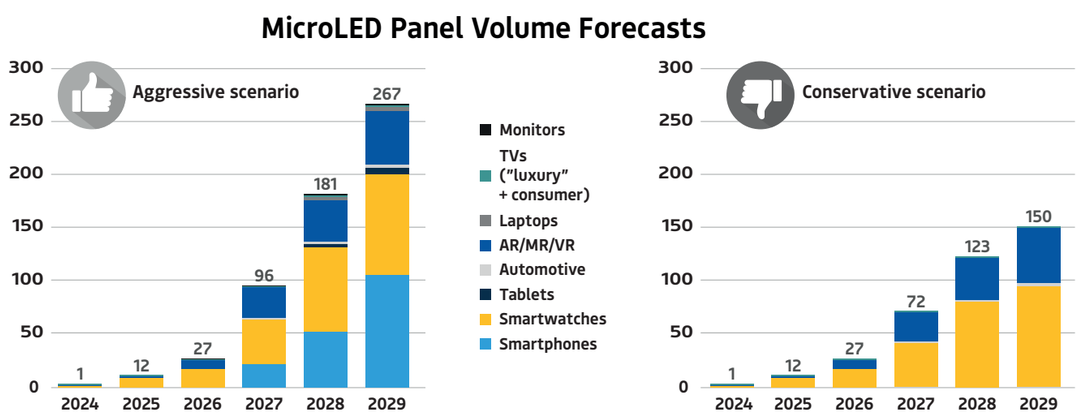


*Figure 4: MicroLED Panel Volume Forecasts. Source: MicroLED report, Yole Intelligence, 2022*

# PHOTONICS NEWS



“Light has been a fascinating field of interest for many generations since scientists first tried to understand its very nature. Today it is used not only for illumination but also for applications like measuring distances, smart sensing and increasingly to transport information. A new and even more challenging trend is to use light as a substitute for electrons. Within BU Photonics we look to exploit new opportunities for light as we work on wafer level optics and smart glasses solutions.”

**Dr. Volker Wuestenhagen**
Head of BU Photonics

# SEEING THE WORLD IN A NEW WAY –

## Welcome to Augmented Reality!

**Once it was the laptop, now it's the smart phone... but watch out... there is a new kid in town as Augmented Reality looks set to be the new mobile computing platform. Evatec's Senior Product Marketing Manager, *Silvio Nigg* and Strategic Marketing Manager, *Majid Sarhangi* introduce different Smart Glasses technologies and the cost effective thin film coating solutions on 200 or 300mm required for mass market application.**

### AR, VR or MR?

Lets begin by reminding ourselves about the differences between all these new emerging technologies. Augmented Reality (AR) adds digital elements to a "live view", typically through a pair of smart glasses, often using a microprojector mounted on the glasses which brings additional information about the real world to the user. Virtual Reality (VR) implies a complete immersion into experiences that shut out the real world, a technology enjoyed by many teenagers and parents around the world as they spend hours using some of the latest gaming technology headsets. The Mixed Reality (MR) experience combines elements of both – live view interacting with digital objects. Microsoft's HOLOLENS™ is a technology used by Evatec's customer service department for remote support – everything from tool breakdown to training is a typical example. According to industry analysts like Yole Group (see pages 82 & 83), 2023 looks like being the start of take off as OEMs start production for professional applications in larger volumes with consumer applications driving growth later in the decade.

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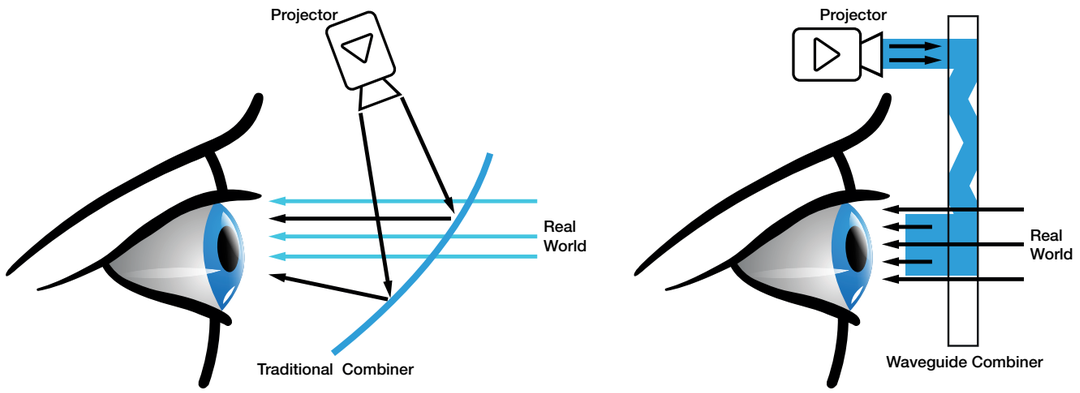



*Figure 1: Comparison of traditional and waveguide combiner for Smart Glasses applications*

## Technologies for AR / MR

Until now the market has seen a range of different display technologies in development for AR/MR applications including "video see through" displays where the user has no direct sight, but also the more familiar "Optical see through display technology "where the user may feel more comfortable and which seems likely to be dominant. Such "see through" displays also rely on integration of a suitable combiner, but even here there is a choice of different technologies between "regular" and so called "waveguide" combiners with potential trade-offs according to image quality, physical bulk of the optics / wearability and ease of manufacture. A better image quality and larger field of view is easier to achieve in a regular combiner approach than in a waveguide solution. However, it comes with the trade-off of device becoming bulkier and pictures being less crisp and detailed. To overcome the trade-off and limitations of the regular combiner approach, waveguide solutions are becoming increasingly popular for smart glass manufactures (Figure 1).

Figure 2 illustrates two different approaches to waveguide combiner manufacturing. In so called "Reflective Waveguides" (Figure 2a), partially reflective mirrors are embedded within the lens. In Figure 2b we see a "Diffractive Waveguide" with Surface Relief Grating (SRG) and Figure 2c a "Diffractive Waveguide" with Holographic grating.

In SRG waveguide-based combiners, when the light rays from the micro projector encounter the input grating, the light dispersed is confined and moves longitudinally through the glasses due to the high Refractive Index of the glass. As the Refractive Index of glass gets higher, the light can propagate at a larger angle range by Total Internal Reflection (TIR) and hence a larger field of view is possible. At the output grating light will be diffracted out of the waveguide and released to our eyes.

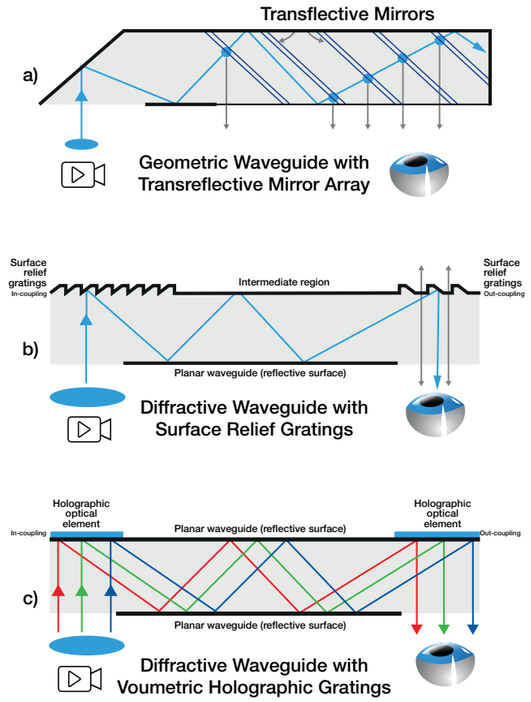



*Figure 2: Categories of waveguide technologies.*



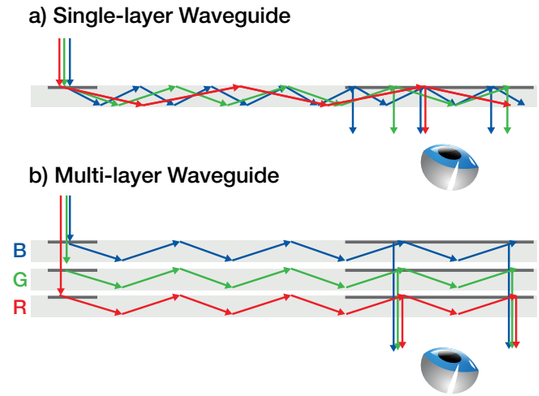
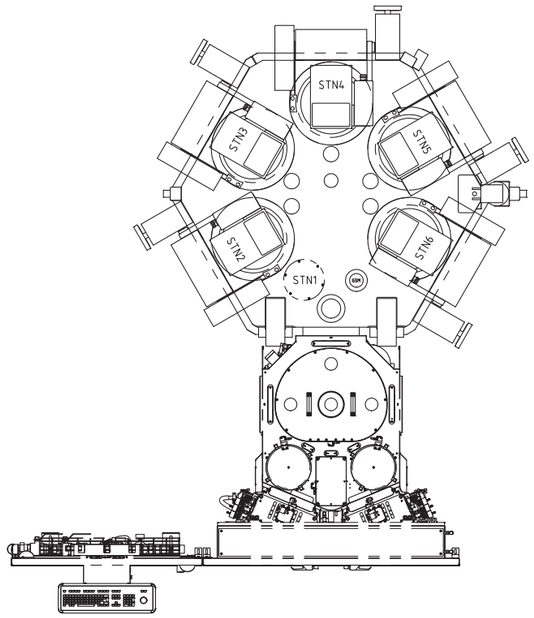



*Figure 3: Comparison between Single and Multi-Layer Waveguides*

Dispersion effects due to the differing wavelengths of red, green and blue have to be controlled to ensure the best colour uniformity and avoid so called "rainbow effects". The most common solution in SRGs is to use two or three layers of waveguides (Figure 3) for red, green and blue colour bands respectively, each layer having its own grating parameters optimized for one colour only.

In determining which choice of waveguide technology is the right one, and its practical implementation in the end product, manufacturers need to consider not only optical performance issues such as field of view, display resolution and colour uniformity but also more subjective factors including wearer design comfort, and the user's "sense of immersion". Overcoming any styling limitations in an image conscious world plus ease and cost of manufacture will also be paramount in enabling the expected transition from professional to consumer applications.

> "Whichever direction the industry and technology take us, it's an exciting time to be in Augmented Reality."



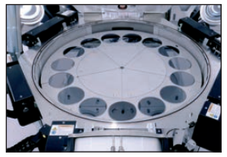



*Figure 4a: Typical CLUSTERLINE® 200 BPM layout. Additional Single Process Module and or substrate flip modules could be added if required. Inset image shows the inside of a batch module.*

## Coatings solutions for waveguide combiners

Reflective combiners typically call for beamsplitter and antireflection coatings. The metals and dielectrics required can be deposited by evaporation or sputter to help generate high image quality and large field of views for which such combiners are known. Diffractive waveguides often call for single layer dielectric or metallic films in addition to the antireflection coatings required to achieve a wide field of view on the high index glass used.

## 200mm – proven performance

The need for longer term cost down looks set to drive the industry to fully automated cassette to cassette solutions. Figure 4a, shows the layout of a fully automated 200mm sputter tool equipped with batch process module enabling integration of up to 4 sputter sources and a plasma source suitable for either dielectric or metal coatings. The cassette to cassette tool also lends itself well to the potential cost savings available for a wafer level coating approach. Proven production performance with high levels of process repeatability and low particles for other existing applications in photonics and optoelectronics have shown that the tool can deliver the costs savings required for high volume production.

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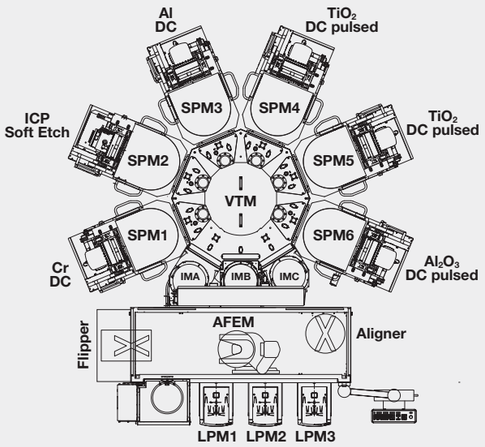



### Vacuum TM

**Up to 6 process modules**

- ✓ PVD Sputter
- ✓ PVD Multisource
- ✓ ICP Soft Etch (arctic)
- ✓ Degasser

**Drop in ports for 3 IMs**

- ✓ Air-locks
- ✓ Active vacuum buffer (optional)
- ✓ HP-or Lamp Degas (optional)
- ✓ Cooler

### Atmospheric Front End

- ✓ LPMs / Robot / Aligner
- ✓ Atmospheric Batch Degas (optional)
- ✓ Buffer / Wafer Flipper (optional)

*Figure 4b: CLUSTERLINE® 300 configured for waveguide applications*

## 300mm solutions are here too

For those manufacturers looking to 300mm processing already, we are excited to be able to offer a 300mm cluster tool too. A typical layout of Evatec's production proven CLUSTERLINE® 300 is shown in Figure 4b.

The single process modules can be equipped for deposition of metals or dielectrics with Front End robot and flipper station making for easy implementation of double sided coatings and cassette to cassette automation. Such tools have already proven themselves in the semiconductor and optoelectronics industries over many years and are ideal to achieve the high layer thickness uniformities, low particle levels and high quality optical films required to drive down costs on 300mm. A selection of performance results for the metal and dielectric films required in waveguide application are illustrated in Figures 5a, 5b & 5c.

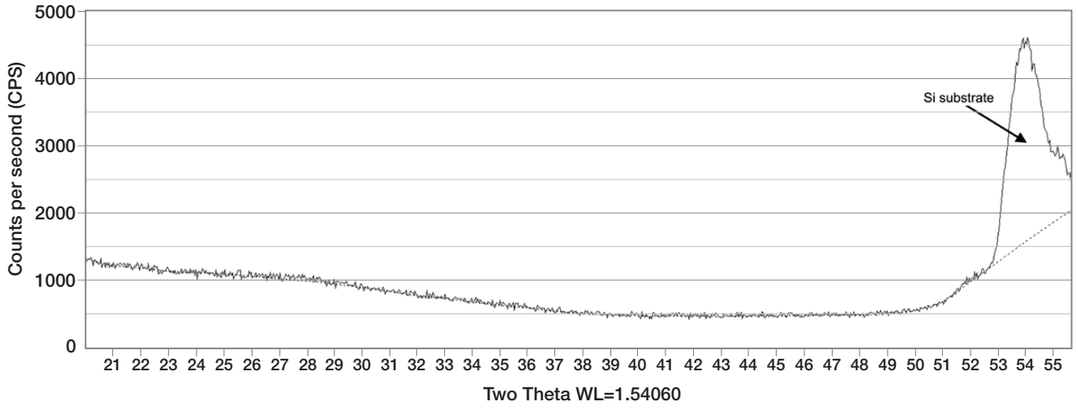



*Figure 5a: Grazing Incidence x-ray diffraction (GIXRD) for a 100nm $TiO_2$ layer on Si substrate*

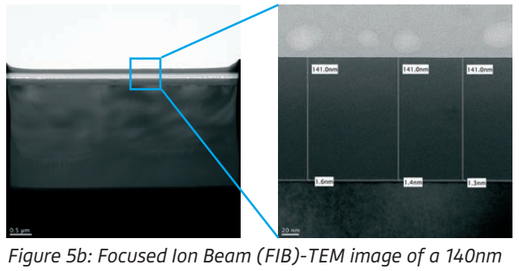


*Figure 5b: Focused Ion Beam (FIB)-TEM image of a 140nm $TiO_2$ layer*

*Figure 5a: No $TiO_2$ peak can be observed showing layers are fully amorphous*

*Figure 5b: Image confirms amorphous structure for a layer deposited on CLUSTERLINE® 300*

*Figure 5c: Excellent particle performance for $TiO_2$ deposition on 300mm*

*Figure 5d: AR coatings on 300mm easily satisfy reflection specifications*

*Figure 5e: Al deposition shows good side and bottom coverage*



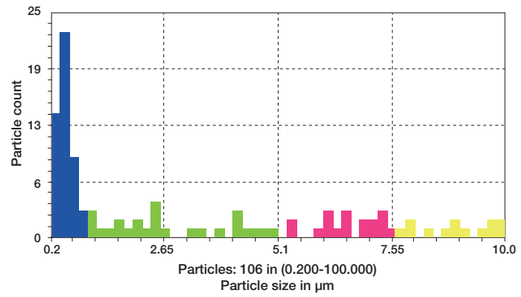



*Figure 5c: Adders for a 100nm $TiO_2$ layer deposited on CLUSTERLINE® 300*

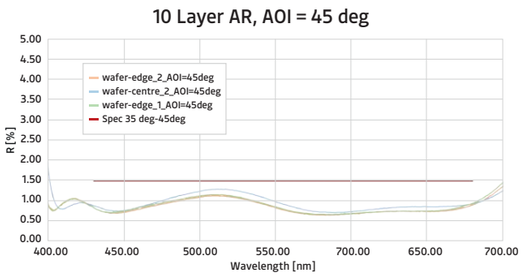
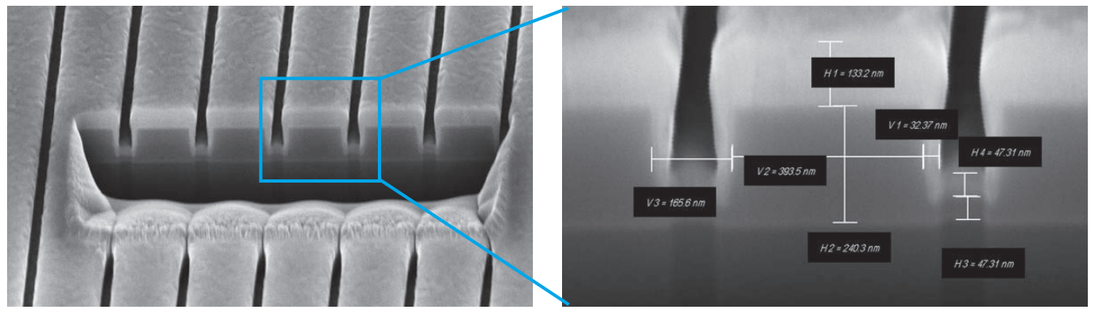



*Figure 5d: Optical performance for 10 layer AR coating on 300mm*




| Period | ~ 165 nm | Pattern Ratio (W/H) | ~ 0.66 |
|---|---|---|---|
| Structure Height | ~ 250 nm | Coating Ratio (Side/Bottom) | ~ 0.68 |
| Bottom | 47.31 nm | Coating Ratio (Side/Top) | ~ 0.243 |
| Sidewall | 32.37 nm | | |

*Figure 5e: Focused Ion Beam (FIB) SEM images of Al deposition on 300mm*

### Finding the right solution for you – Evatec is your partner

In the end every manufacturer is unique with their own product specifications and manufacturing fab integration needs. For some manufacturers with long experience, the flexibility and precision of evaporation remains a key advantage, but for others, the way in which sputter lends itself to full cassette to cassette automation more easily is the driver for delivering the lower manufacturing costs they need. In some cases manufacturers may prefer to work at smaller substrate sizes, where the flexible mini batch carrier handling of different form factors, or full 200mm wafer handling on Evatec's CLUSTERLINE® 200 BPM gives them complete production flexibility. In other cases, the drive to a wafer level approach on the largest substrates possible will make CLUSTERLINE® 300 the tool of choice. ◻

> “Process solutions are now ready on both 200 and 300mm according to customer needs”

# A view from Yole Group

## A status on AR headsets

### From the players to the technology

Major players are fighting it out. Every company is pushing to make consumer AR a reality. Facebook signing an exclusive deal with Plessey for a supply of microLED microdisplays for AR illustrated the interest in this new display technology. In early 2022, we saw Google acquiring Raxium, a microLED company, for a reportedly estimated $1 billion. Interestingly, they also acquired the IP of Jasper Display, a company providing backplanes for microdisplays to accompany that.

This mainly shows two things:

- Firstly, Google has been more and more assertive, trying to catch up, proving that we are getting closer and closer to AR happening. This is not at too far out of sight.
- Secondly, one cannot consider only microLEDs by themselves: backplane technology is of utmost importance, and Snap's acquisition of Compound Photonics is yet another sign of this.

With Snap, ByteDance, Meta, Google and the likes becoming even more engaged, and with the 2023 milestone in mind, we understand that AR is becoming a major strategic zone for everybody. The strategies are however completely different. While Snap and ByteDance are content providers, Apple or Sony do everything as well as creating their own content with a clear roadmap, and Meta is not yet benefitting from such a rich ecosystem. This is all globally a battle driven by the major players with smaller technology providers also trying to make an impact. According to Yole Intelligence, the supply chain is setting itself up in line with expectations of a tipping point in the AR market during 2023. The first generation of headsets show limited capabilities, and glasses with acceptable performance and form factor with the disruptive technologies are only expected around 2023-2024, once the OEMs start shipping. They will probably be expensive and at low volumes, but will make a statement for a brand, and serve as an important taster for testing the market.

### Technology status

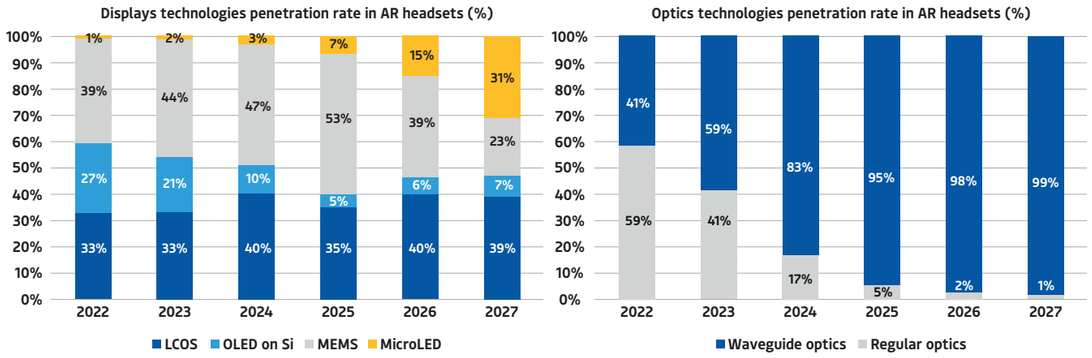
To make it to market in these timescales, the technological ecosystem is still open and is shaping itself around new technologies for which manufacturing issues have not yet been solved. Many technological difficulties have still to be overcome, for there is no bypassing the laws of Physics. At Yole Intelligence, we consider the optical engine as the display engine and the optics associated. For the former, incumbent projection technologies have been chosen (LCOS, DLP) for lack of a better choice so far which are still bulky, and not providing an acceptable form factor for the consumer. For the later, OLED on Si cannot deliver the required brightness for day-to-day live use case with acceptable optics, whilst the microLED dream also continues. MicroLEDs could theoretically deliver the desired level of performance with an acceptable form factor, although much effort is still needed to improve efficiency, light extraction, driving compensation, color conversion and so on. JBD is shipping products, proving that microLEDs are not only a promise, and the recent acquisition of Raxium by Google brings even more light to the technology.

LBS, "pushed" or "brought to the forefront" by Microsoft with Hololens 2, has been trying to carve out a way to exist, further promoted by ST Microelectronics and their partners from the LaSAR Alliance. According to Yole Intelligence, LBS will serve as a transitory technology that will help OEMs to wait for the full color single panel microLEDs to become a reality. However, LCOS will still be the go-to technology at first, especially with the strong efforts around making them less bulky (Magic Leap, Avegant).

In the meantime, for the optics, we are of the opinion that these will be based on waveguides for the greater part, as they provide the form factor the consumer is asking for. Work continues on improving their performance in terms of FOV and efficiency, but it looks like an acceptable level has now been reached.

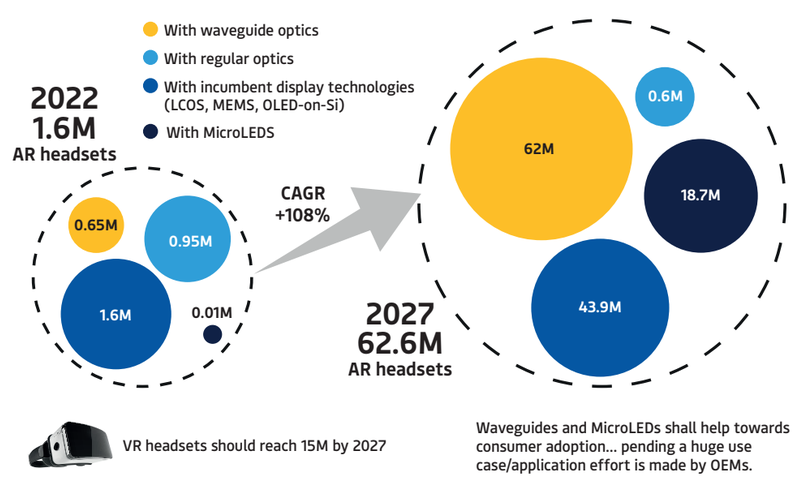
Is the bigger challenge now around reducing the cost of going towards glass panels with the fusion process? ◻

### AR forecasts – Technology splits




*Source: Displays and optics for AR & VR report, Yole Intelligence, 2022*

### AR & VR forecasts - Headset volumes




*Source: Displays and optics for AR & VR report, Yole Intelligence, 2022*

### Players positioning


*Source: Displays and optics for AR & VR report, Yole Intelligence, 2022*

**About the author**

**Zine Bouhamri, Ph.D**, is Team Lead Analyst, Imaging & Display activities at Yole Intelligence, part of Yole Group. He is managing the expansion of the technical expertise and the market know-how of the company.

In addition, he actively assists and supports the development of dedicated imaging and display collection of market & technology reports and monitors, as well as custom consulting projects.

Zine Bouhamri holds an Electronics Engineering Degree from the National Polytechnic Institute of Grenoble (FR), one from the Politecnico di Torino (IT), and a Ph.D. in RF & Optoelectronics from Grenoble University (FR).

# EDGE EMITTING LASERS – manufacturing challenges for new markets

Evatec's Senior Product Marketing Manager, ***Dr. Clau Maissen***, talks about production solutions for the antireflection and high reflectivity coatings needed in emerging applications for Edge Emitting Lasers (EELs).

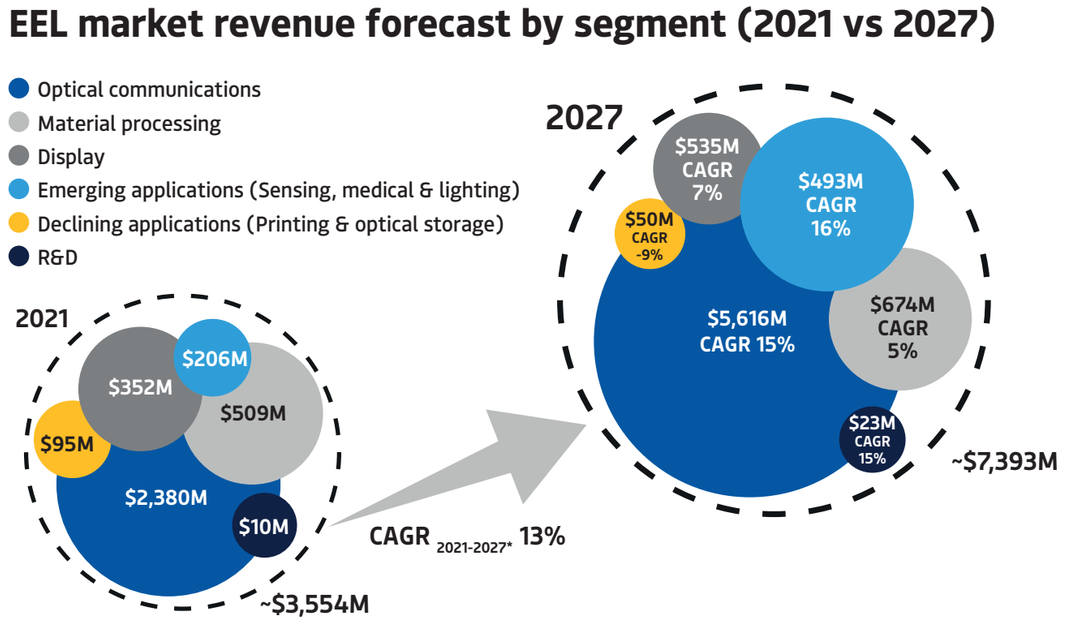



*Figure 1: Expected growth of EEL market. Source Edge Emitting Lasers report, Yole Intelligence, 2022*

## New opportunities in optical communication

With long established applications including optical data storage and material processing, the market for laser diodes may not be new, but opportunities in growth areas like new optical communication applications and autonomous driving are setting manufacturers challenges in delivering effective thin film manufacturing solutions for new diode materials and at much larger volumes (see Figure 1).

## How are thin film coatings used?

Figure 2 shows the typical construction of an edge emitting laser where light output from the active region must be maximised using antireflection coatings at the front side, while unwanted output / losses from the backside must be minimised by use of a high performance mirror.

Coatings designs and deposition processes for the required antireflection and high reflectivity layers must be optimised according to laser diode materials and emission wavelengths. Besides the spectral requirements, avoiding damage to the sensitive laser device is key for long device lifetimes as required in optical communication applications. Some example laser diode material combinations and corresponding output wavelength ranges are shown in Figure 3. Applications in optical communication use mainly 1.3µm and wavelengths around 1.55µm to match the low-loss window of silica optical fibers and are built on Indium Phosphide or InGaAs.

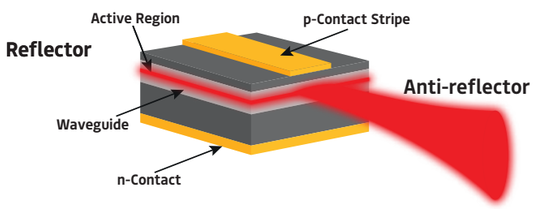



*Figure 2: Schematic of an edge emitting laser diode*

## Optical communications –

| Laser diode material (active region / substrate) | Typical emission wavelengths | Typical application |
|---|---|---|
| InGaN / GaN, SiC | 380, 405, 450, 470 nm | Data storage |
| AlGaInP / GaAs | 635, 650, 670 nm | Laser pointers, DVD players |
| AlGaAs / GaAs | 720-850 nm | CD players, laser printers, pumping solid-state lasers |
| InGaAs / GaAs | 900-1100 nm | Pumping EDFAs and other fiber amplifiers; high-power VECSELs |
| InGaAsP / InP | 1000-1650 nm | Optical fiber communications |

*Figure 3: Most commonly used laser diode materials*



## Coating quality and repeatability is key

Laser manufacturing uses complex semiconductor processes for the active light producing layers. For the final laser diode performance the active layers are crucial but no less important are the passive films like high reflector mirror (HR), antireflection (AR) coating or metallization layers.

In a typical manufacturing approach for laser diodes the HR and AR facet coatings are applied before final dicing into individual lasers. These so-called laser bars are stripes of lasers arranged side by side (Figure 4). Multiple laser bars are bundled into special jigs for deposition of the AR and HR films. Vacuum flipping allows us to coat the AR as well as the HR in a single batch without breaking the vacuum. Maintaining consistency of coating quality across all diodes within a single bar, all bars within a coating batch, and then from "batch to batch" is essential.

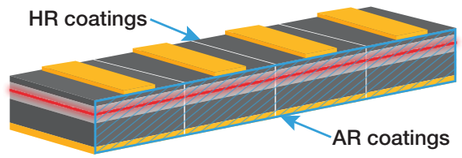



*Figure 4: Schematic view of the semiconductor chip of a diode laser bar*

Some of the typical coating specifications to consider along with example results for sputter coatings performed on Evatec's CLUSTERLINE® 200 BPM are illustrated below.

### 1. Optical performance

Laser diodes are being used in optical communication applications in which ever greater distances and higher data rates are required so coating specifications are more demanding. For the diode output for example, antireflection coating specifications may call for levels of reflectivity less than 0.03% over the target wavelength range. Figure 5 shows the performance of an AR coating on InP against customer specifications.

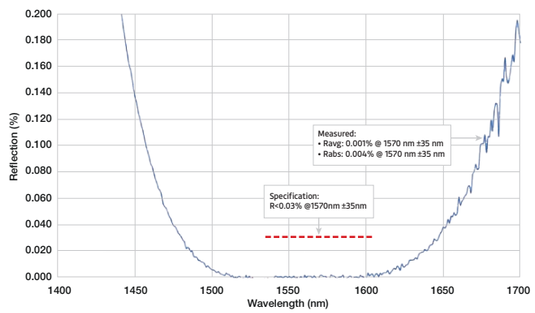



*Figure 5: Optical performance of an AR coating on InP*

### 2. Process stability

Such high levels of optical performance are only effective when process stability can be maintained. Figure 6 shows the typical stability levels batch to batch (11 runs in a row) on InP specified for 1270nm. Figure 7 illustrates the stability of coating process from edge to center of coating jigs.

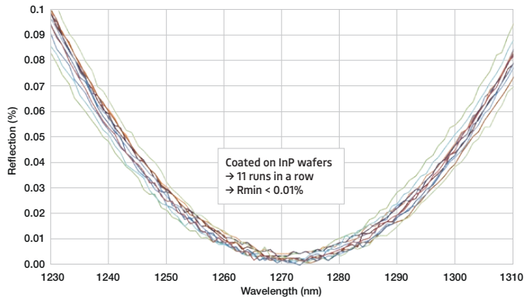



*Figure 6: Process repeatability for an AR coating centered at 1270nm*

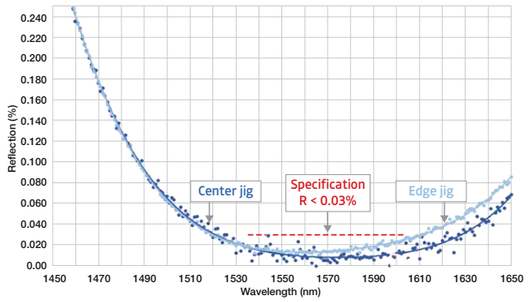



*Figure 7: Stability of coating process designed for 1570nm for jigs placed on the center or at the edge of an 8 inch carrier*

### 3. Laser Induced Damage Threshold

ISO 21254-1:2011 defines the Laser induced Damage Thresholds as "the highest quantity of laser radiation incident upon the optical component / material for which the extrapolated probability of damage is zero". But it's a complex parameter to understand with many detailed studies available in the literature to shed light on damage mechanisms. In general however, threshold values reflect, not only the inherent nature of the material itself, but also the "quality" of the deposited coating with influences from both micro or nano defects within a coating (e.g. voids, inclusions) and from coating interface effects (e.g. surface roughness, particles. Figure 8 show the value for a single layer coating of a typical material like $SiO_2$ measured on Herasil according to ISO norms.

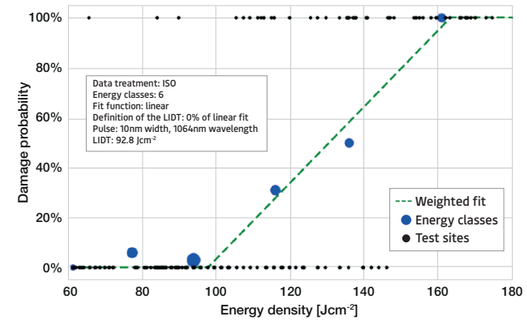



*Figure 8: $SiO_2$ damage probability curve at*

>>>>>

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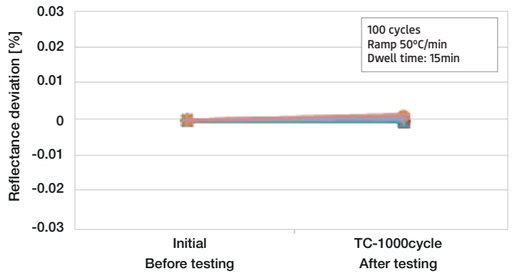


*Figure 9a: Temperature cycle test -60°C to 140°C*

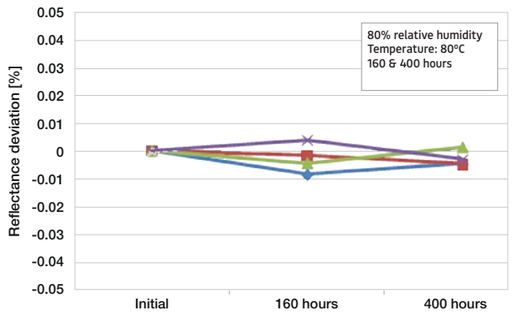


*Figure 9b: High temperature, high humidity test*

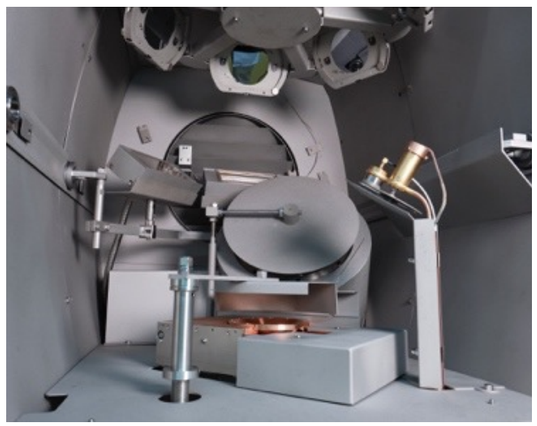

*Figure 10:* Typical BAK configured with "Flexcalotte"
- ARs
- Reflectors
- Metals

## How are thin film coatings used?

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## Optical communications – Coating quality and repeatability is key

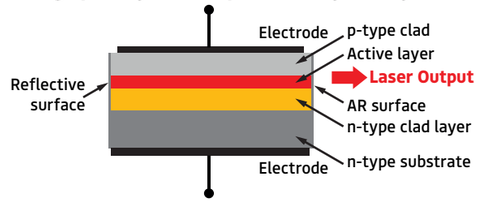



*Figure 11a: Typical EEL cross section showing stack construction*

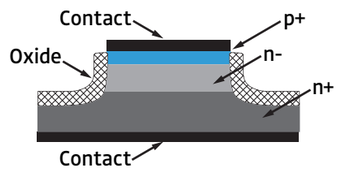
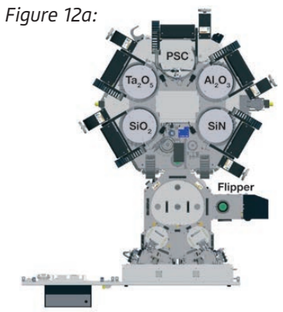


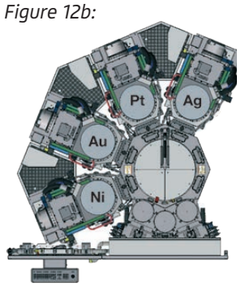

*Figure 11b: Typical 3D mesa structures in some EEL*

*Figure 12a:*




CLUSTERLINE® 200 BPM
- ARs
- Reflectors

*Figure 12b:*




CLUSTERLINE® 200
- Metals
- Passivation



# CLUSTERLINE® 200 BPM –
## When you need 100 million lasers per year

| | | |
|---|---|---|
| **10** lasers per bar | **24/7** Hours per week | **10** Lasersbars per jig |
| **6** Carriers / hour | **20** Jigs / carrier | **100M** lasers per year on one CLUSTERLINE® 200 BPM |

### Want to know more?

If you would like to know more about evaporation or sputter solutions for Edge Emitting Lasers or any of the results presented here please contact your local Evatec Sales and Service or complete our web enquiry form at **www.evatecnet.com/about-us/contact-us/**

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