

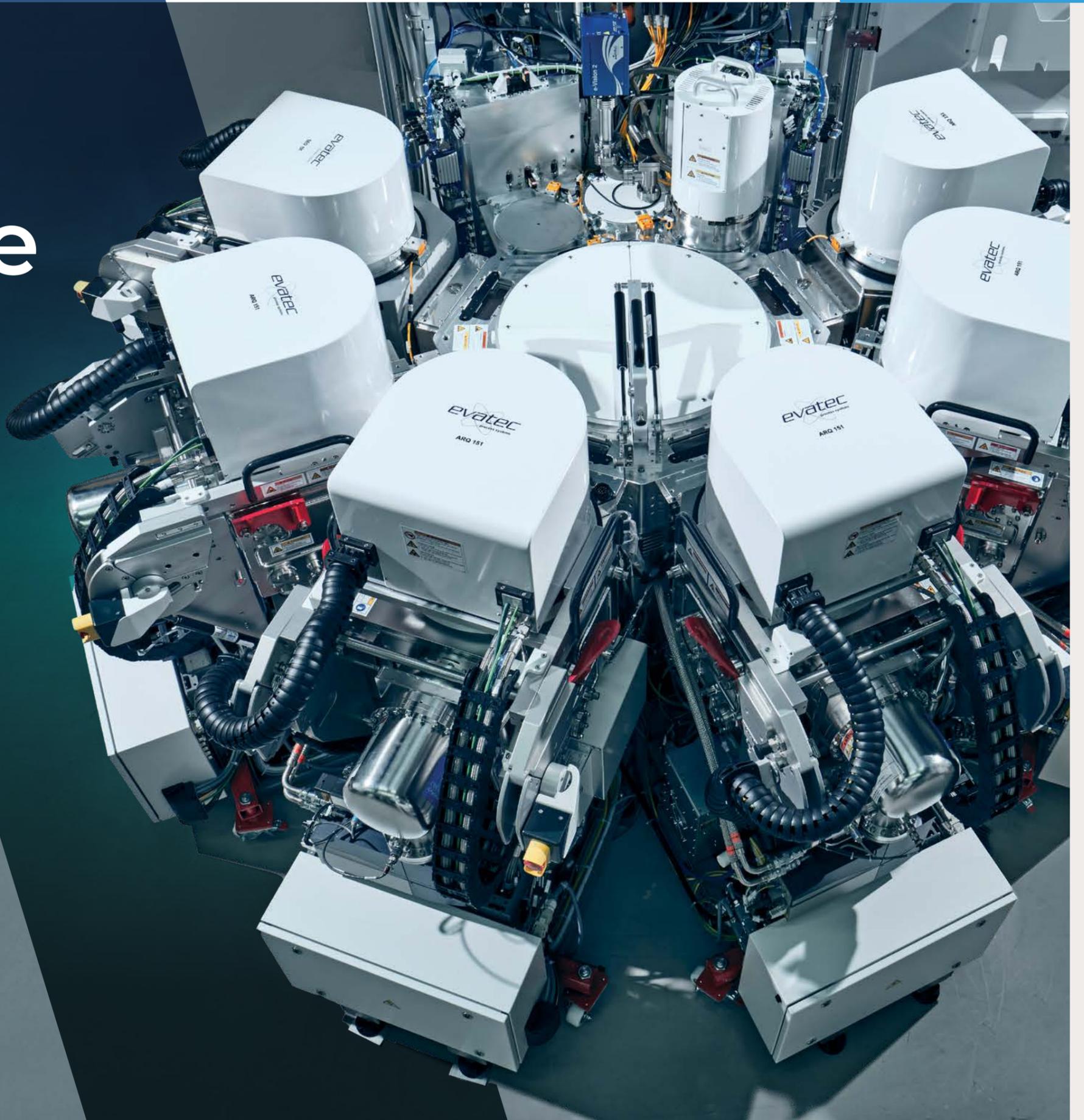


Powering the SiC Future

How Evatec's CLUSTERLINE® 200 empowers next generation MOSFETs



Dr. Yuan Lu, Evatec China's Manager of Technical Marketing Management, shares how the CLUSTERLINE® 200 is empowering customers in 200 mm SiC power MOSFET production through a proven platform and local service support.



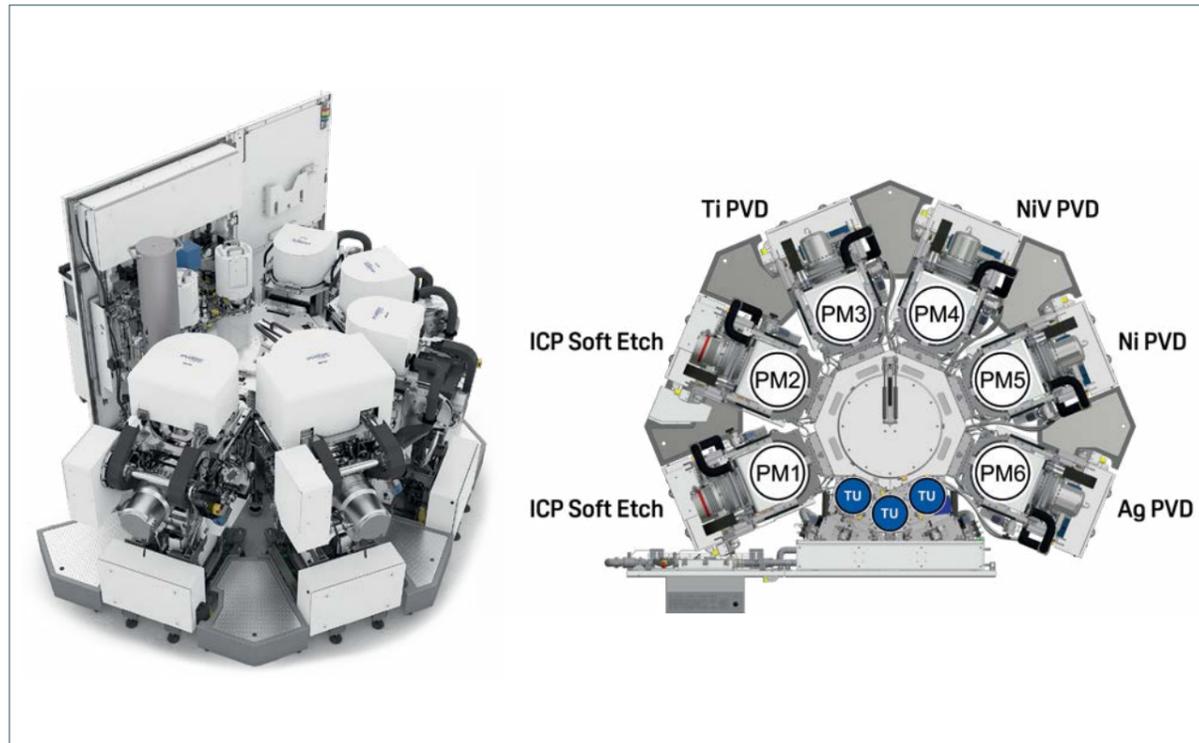


Figure 1. Left: CLUSTERLINE® 200 Platform.

Right: Configuration of CLUSTERLINE® 200, equipped with 6 SPM with 6 TU modules, perfect for BSM, STM and Silicide.

Silicon Carbide (SiC) has become a strategic enabler for the transition to high-efficiency power electronics, with SiC MOSFETs driving advances in electric vehicles (EVs), renewable energy, and industrial power systems. Compared with traditional silicon devices, SiC MOSFETs deliver lower switching losses, higher breakdown voltage, and superior thermal performance.

The domestic EV industry in Asia is the primary driver, and demand is forecast to keep expanding at double-digit rates. SiC MOSFETs are increasingly integrated into traction inverters, onboard chargers, and DC/DC converters to extend range and enable fast charging. To meet this demand, global leaders and local players are investing heavily in Asia. STMicroelectronics, Infineon, and Wolfspeed have partnered with local foundries and assembly houses to accelerate SiC adoption in the EV supply chain.

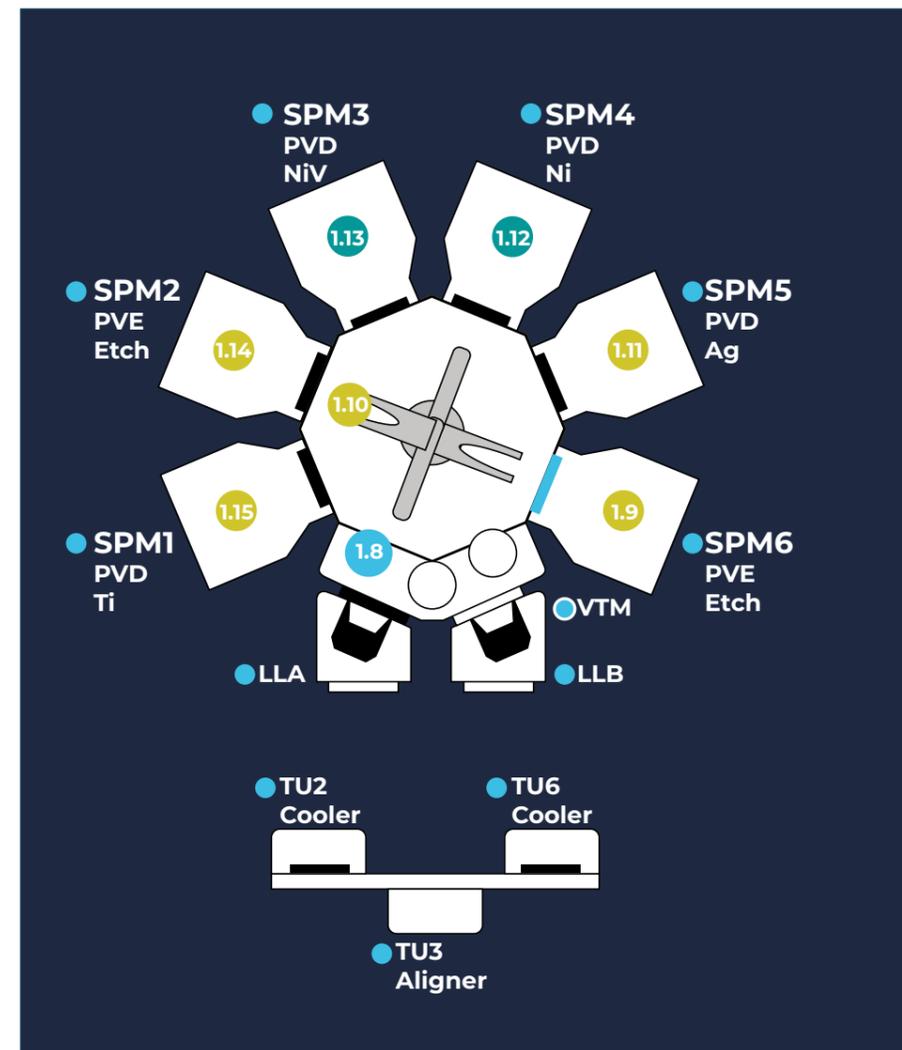
These collaborations, ranging from joint ventures on wafer production to localized device packaging, help transfer process know-how while supporting domestic capacity growth. At the same time, IDMs such as Sanan IC, HHGrace, BYD Semiconductor, and InventChip are scaling 6-inch lines and preparing 8-inch SiC pilot lines in provinces like Hunan and Fujian. The move toward 8-inch wafers is expected to bring cost reduction and volume scalability.

Within this ecosystem, metallization steps are essential. Ti and Ni layers form ohmic contacts and silicides, backside metals provide thermal management, and Ag-based solderable tops enable reliable interconnection. As the SiC industry enters the 8-inch era, advanced PVD tools capable of depositing Ti/Ni(Ni)/Ag stacks with high throughput, uniformity, and flexibility will be vital to support both local manufacturers and international partnerships driving the EV revolution.

1. Full automation with single process modules

Evatec's solution is its CLUSTERLINE® 200 & 300 family equipped with single process modules (SPM). An example of CLUSTERLINE® 200 is shown in Figure 1. Unlike traditional batch systems, the SPM architecture provides complete flexibility in configuring ICP etch, Ti, Ni, NiV, and Ag deposition modules on one platform. This eliminates cross contamination between metals, a critical factor in SiC MOSFET frontside and backside metallization where adhesion layers, ohmic contacts, and solderable tops are integrated in a single flow.

Moreover, the creative TU (Treatment Unit) design enables customers to integrate functions such as degas, cooling, RGA (Residual Gas Analyzer), wafer alignment, and dummy wafer storage in the transfer module without occupying the chamber slot.



Flow steps

- ▼ Step #1 (Aligner) default
- ▼ Step #2 (Exclusive) SPM_SPM2 SPM2_NtveOxRmvl
- ▼ Step #3 (SPM_SPM1) SPM1_Ti
- ▼ Step #4 (SPM_SPM3) SPM3_NiV Step #5 (SPM_SPM5) SPM5_Ag
- ▼ Step #6 (Exclusive) TU_TU26 TIOG AA AGAA

Figure 2:

Left: Intuitive Evatec eXperience Operation GUI, configured a PVD equipment for BSM, STM and Silicide processes.

Right: Process flow design for BSM process.

The different metallization process types are clearly defined within Evatec's CLUSTERLINE® 200/300 platform:

- **BSM (Backside Metallization):** ICP/Ti/Ni(NiV)/Ag stacks designed for solderable and thermally conductive backside contacts
- **STM (Solderable Top Metallization):** ICP/Ti/Ni(NiV)/Ag stacks optimized for robust front-side interconnects
- **Silicide Formation:** Ti or Ni deposition for ohmic contacts, enabling low-resistance interfaces
- **Optional FSM (Frontside Metallization):** ICP/Ti/TiN/AICu stacks featuring up to AR 5:1 trench fill capabilities

A single CLUSTERLINE® tool (Figure 2) can be configured to handle BSM, STM, Silicide, and FSM modules simultaneously, giving customers maximum flexibility in their device roadmap. This is enabled by a specially designed modular chuck, which satisfies the no-scratch requirement essential for BSM processes on thick and sensitive SiC wafers, while also

being robust enough to support STM and Silicide processing. Moreover, the architecture allows for additional ICP etch chambers to be configured, providing in-situ surface cleaning or etch capability before metallization.

Each module offers precise wafer handling, cassette-to-cassette automation, and state of the art recess chuck technology, ensuring wafer safety and process repeatability. For customers, this translates into stable film uniformity across 200 mm substrates, tighter process windows, and straightforward recipe fine tuning for new device generations. Furthermore, single process modules inherently require fewer clean parts compared with batch chambers, which reduces maintenance downtime, lowers consumable costs, and ensures longer mean time between cleans. This balance of flexibility, performance, and reliability sets the Evatec platform apart for power device fabs moving into 8-inch SiC. Process performance data is reported in Figure 3.

Stack	SPM	Rate	Uniformity 1sigma	Stress MPa
Pre Clean	SPM2 + SPM6	400 A/min	6.13%	~-300
Ti	SPM1	40 A/s	1.8%	~50
NiV	SPM3	130 A/s	1.4%	~200
Ag	SPM5	95 A/s	1.99%	~0
Cool	TU2 + TU6			

Figure 3: Real process sampling data for ICP/Ti/NiV/Ag process flow, result in 35.1 wafer/hour on 8-inch SiC applications.

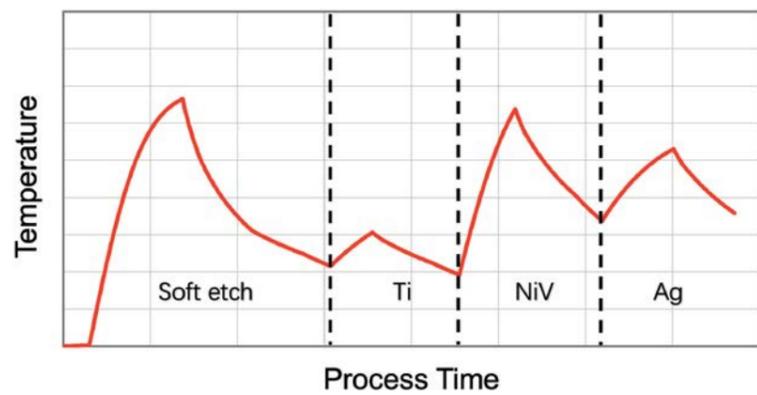


Figure 4: A typical simulation sample that Evatec will provide to estimate the process maximum temperature, throughput according to substrate and layer stack information.

2. Process temperature simulation capability

Another critical advantage is the ability to simulate process temperature conditions before a tool is even installed at the fab (Figure 4). By modeling the substrate type, wafer thickness, and target layer stack, engineers can calculate peak wafer temperatures at specific deposition rates and then correlate these with wafers-per-hour (WPH) throughput.

This unique service enables customers to predictively evaluate their process integration flow, avoiding surprises during ramp-up. For example, in high-aspect-ratio metallization or backside deposition on thick SiC wafers, process thermal budgets are tight. Simulation demonstrates how throughput and deposition rates influence peak wafer temperature, ensuring that neither R_c degradation nor film stress compromises device performance.

Customers gain a detailed understanding of process limitations and opportunities during the evaluation stage, accelerating decision-making and shortening time-to-market.

“Evatec doesn’t just deliver hardware – it delivers actionable process intelligence that de-risks investment and guarantees optimized production from day one.”

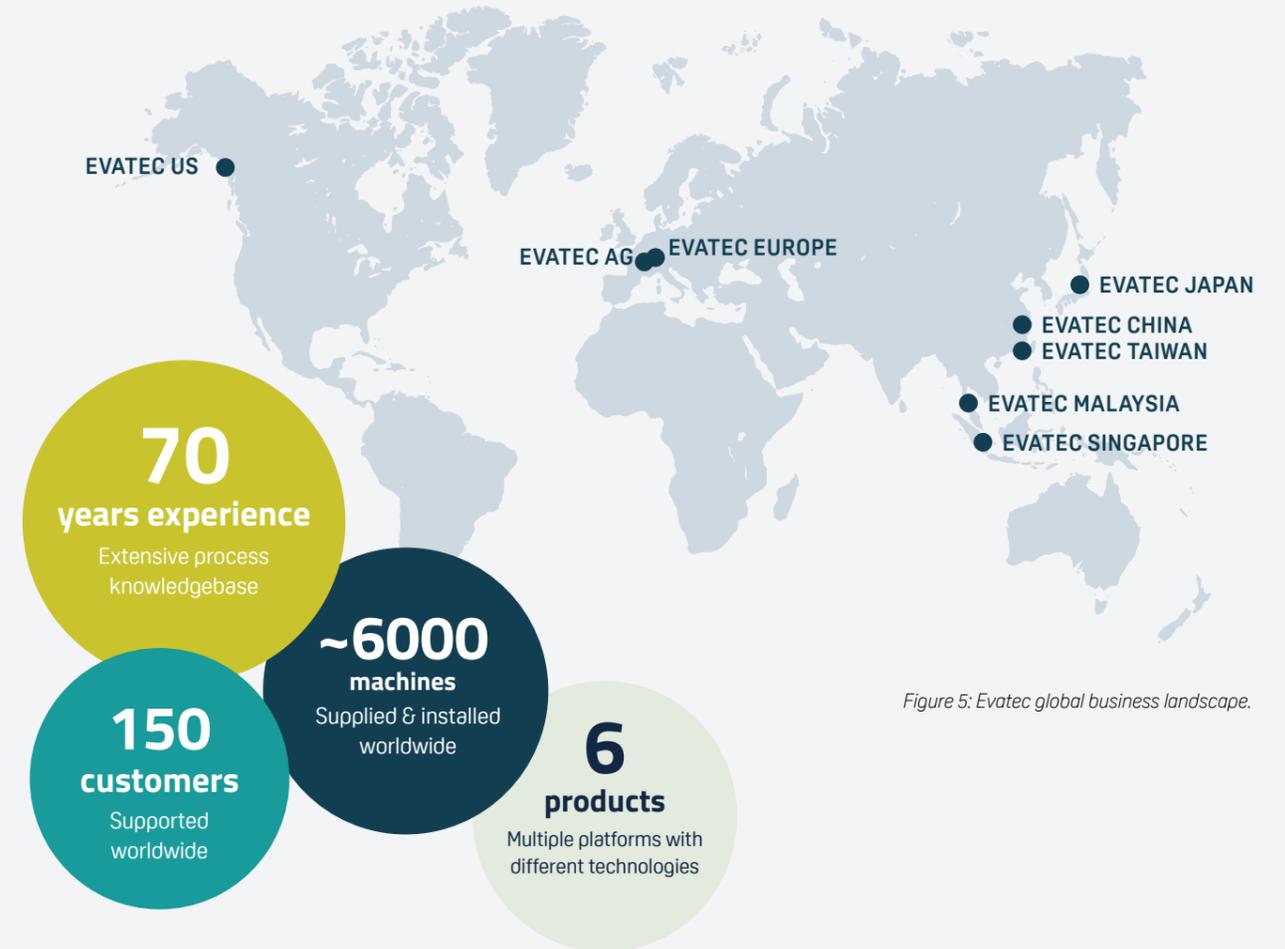


Figure 5: Evatec global business landscape.

3. A strong Customer Service team – from local offices to headquarters

Equally important to technology is the service infrastructure supporting it. As part of its global Sales and Service Organization (Figure 5), Evatec has invested heavily in its Asia operations since 2017, building a dedicated group of around 100 semiconductor professionals. These engineers and managers are well-educated, with backgrounds spanning process, software, and hardware disciplines.

Their mission is to provide fast, professional responses to Asia customers, from OSATs and IDMs to emerging SiC device makers. Service offerings include installation, troubleshooting, performance optimization, and critically design

of experiments (DOE). DOEs can be coordinated directly with the headquarters in Switzerland for advanced cases or designed and executed locally to ensure the fastest reaction speed in tackling customer challenges.

This hybrid model gives fabs direct access to Evatec’s global process expertise while maintaining the agility of a local support team. Customers therefore benefit from rapid turnaround during qualification and production ramp, minimizing downtime and ensuring maximum equipment utilization. The presence of spare parts warehouses, technical training, and an Asia Technical Task Force (ATTF) further strengthens Evatec’s ability to deliver world-class service in the region.

Conclusion

The combination of single process module flexibility, predictive temperature simulation, and an experienced local support organization makes Evatec the partner of choice for fabs scaling to 8-inch SiC MOSFET and power device production. As international and domestic players push to secure leadership in EV, renewable energy, and industrial power markets, Evatec’s CLUSTERLINE® platforms provide the process stability, transparency, and service responsiveness required for success. By uniting Swiss engineering precision with Asia service strength, Evatec ensures that customers can confidently meet the demands of next-generation power electronics with the lowest cost of ownership and highest reliability.