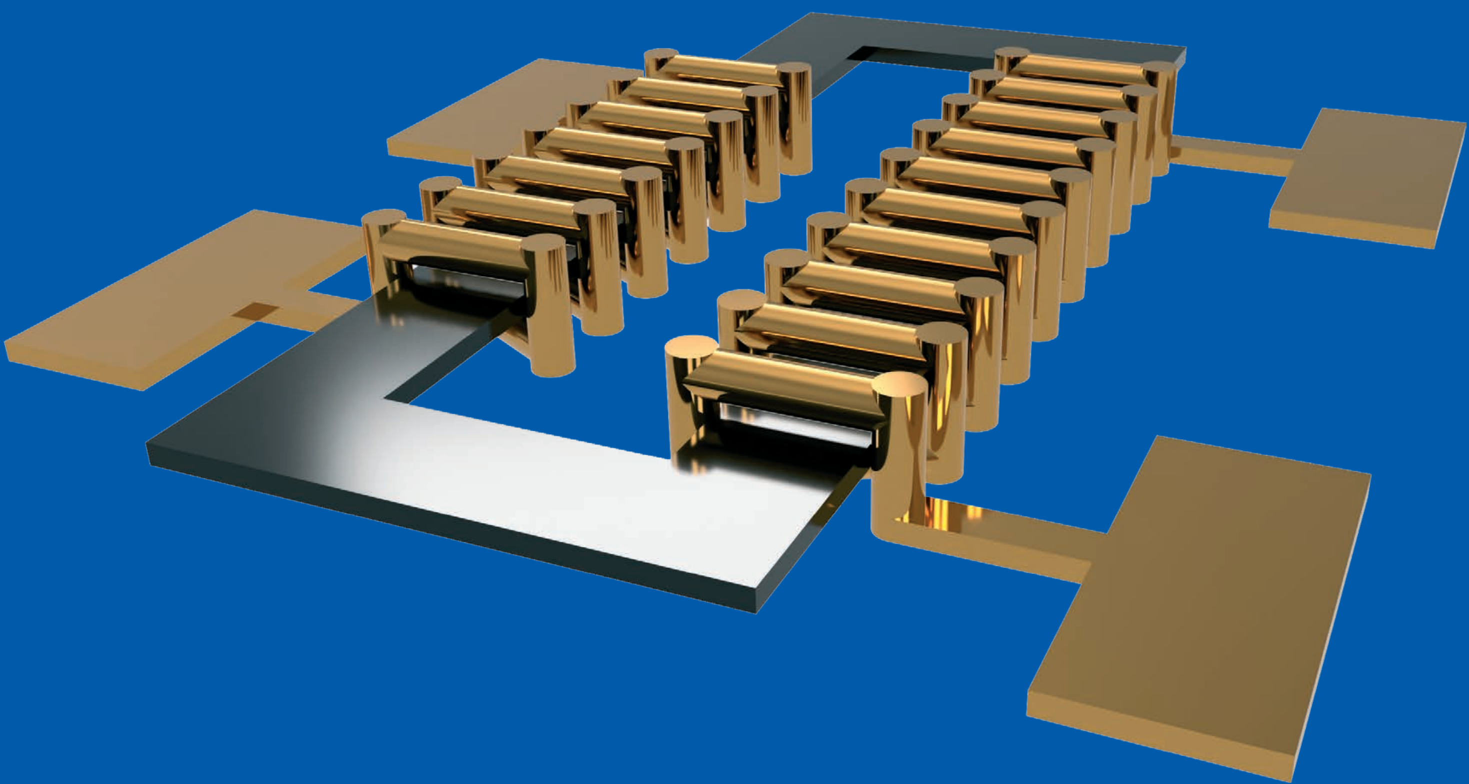
BREAKTHROUGH IN THIN FILM BASED INTEGRATED MAGNETIC PASSIVE DEVICES FOR RF APPLICATIONS

The integration of on-chip passive devices (e.g. inductors and transformers) with magnetic materials into silicon technology has been for decades a major challenge in the move towards monolithic solutions for wireless communications, RF integrated circuits, power delivery and management, and EMI noise reduction. Senior scientist **Dr. Claudiu Valentin Falub** explains how the LLS EVO II allows engineering of superior soft magnetic multilayers that ultimately led to ultra-low profile integrated magnetic solenoid micro-inductors with record inductance density and quality factor.



Thin-film integrated passive devices (IPD)

Integrated Passive Devices (IPDs) are attracting an increasing interest due to constant needs for lighter, smaller, faster, "smarter", and more economical and sophisticated mobile devices. IPDs are multiple passive components sharing a substrate and a package, which can be designed as flip-chip mountable or wire bondable components, and are generally fabricated on silicon, silicon-on-insulator (SOI), GaAs, sapphire, or glass substrates using standard wafer fabrication technologies, such as thin film and photolithography processing. A variety of functional blocks, e.g. impedance matching circuits, harmonic filters, couplers and baluns, power combiner/divider, etc. can be realised by IPD technology (see Fig. 1).

Inductors and transformers are the passive electrical components that can store energy in the magnetic field created by the current passing through them, and form together with the resistors and capacitors the building blocks of the IPDs. Depending on the final application, there are planar (2D) and 3D inductor designs. The miniaturisation of these components has, however, been a major challenge for decades. Hence, integrated thin film magnetic cores with high magnetic permeability (μ_r) were proposed, since the inductance (L) of magnetic-core inductors (and corresponding solenoids associated with magnetic-core micro-transformers) is proportional to μ_r. Subsequently, Intel demonstrated that planar inductors with magnetic cores can be integrated with 130 nm and 90 nm CMOS processes [1,2]. More recently, magnetic-core 3D inductors were fabricated using CMOS manufacturing equipment and process by Ferric and TSMC [3].

The figure-of-merit (i.e. quality of the inductor) is given by the quality factor (Q), which is a dimensionless number defined by $Q = 2\pi f{\times}L\ /\ (R_{dc} + R_{ac} + R_d)$, where f is the frequency, R_{dc} is the DC winding resistance (winding loss) that scales with the wire cross-section

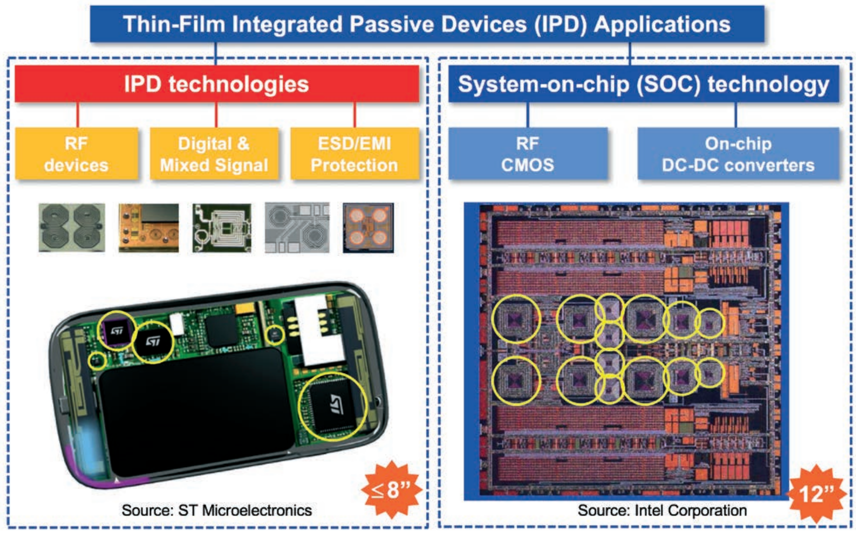


Fig. 1: Applications of the thin-film integrated passive devices (IPD). Left: IPD technologies for telecommunications, e.g. RF, digital and mixed signal devices, and ESD/EMI protection, which are usually realised on 8" or smaller substrates. Some typical IPD devices found in a mobile phone are depicted by yellow circles. Right: complex system-on-chip (SOC) technologies, e.g. RF CMOS and on-chip power converters, which have to be realised on 12" wafers since they need to be compatible with Si CMOS technology. Air-core spiral coils depicted by yellow circles occupy a substantial chip area, illustrating the need to shrink these components for the next generation mobile devices.

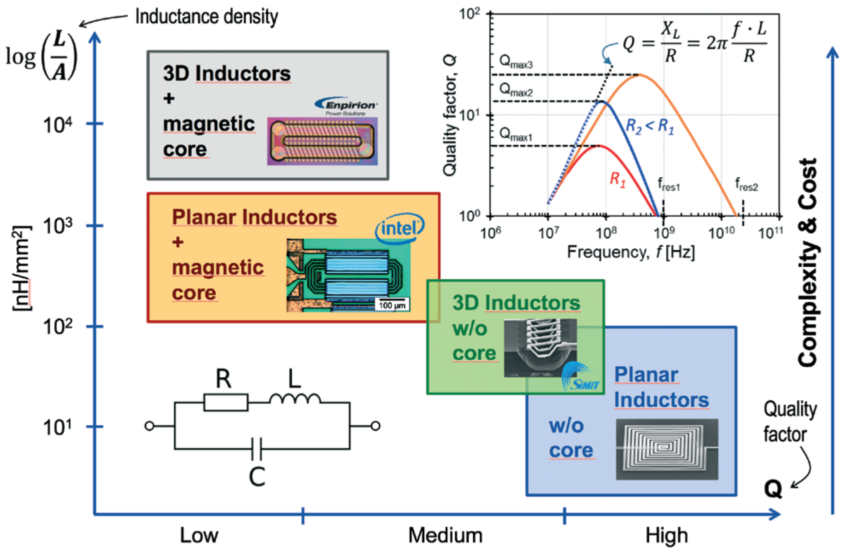


Fig. 2: Ferromagnetic core allows for a much higher inductance density, but the quality factor is reduced due to various losses associated with the magnetic material. The inset in the low left corner shows the equivalent circuit of a "real" inductor, where L is the inductance, R is the series resistance associated with various losses, and C is the turn-to-turn and turn-to-core distributed capacitance. The inset in the top right corner indicates that inductor's maximum quality factor can be increased by either lowering the series resistance (blue curve), or by increasing the resonance frequency (green curve).

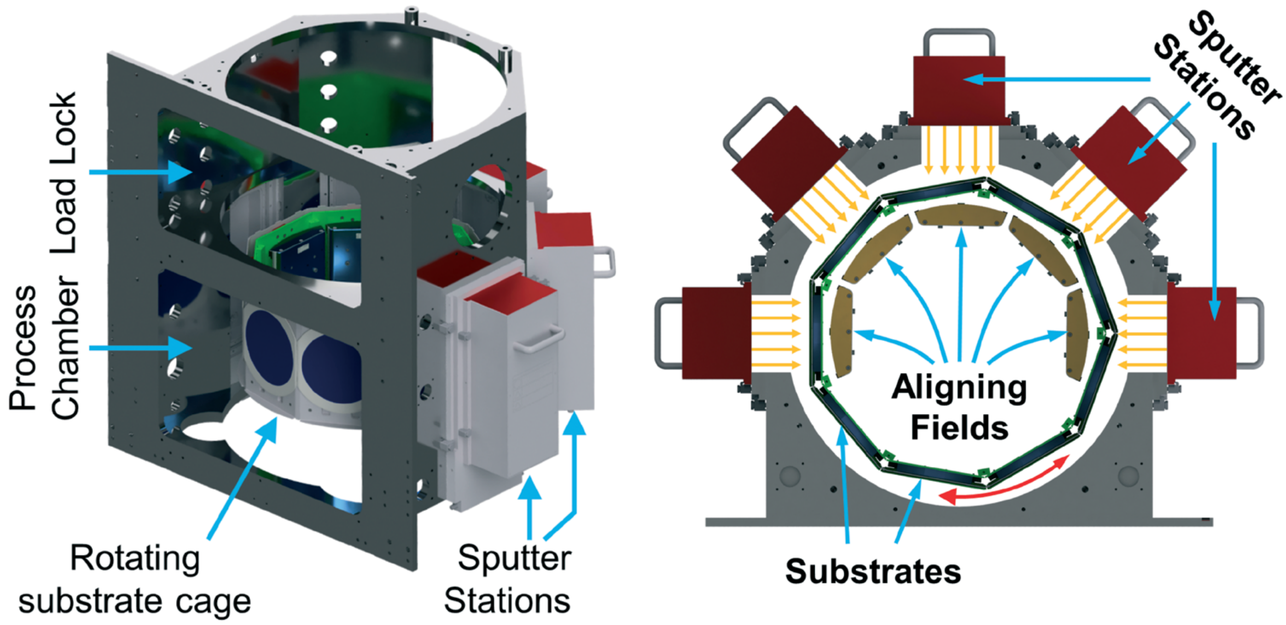


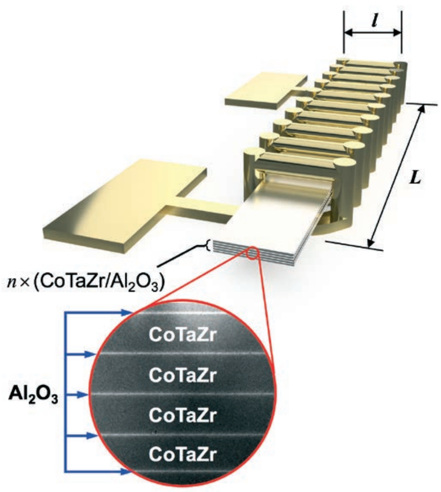
Fig. 3: Schematic diagrams of the LLS EVO II batch sputter system with 5 process modules that can operate, one or more at a time, in order to fabricate thin films based on single or multiple materials. To induce the in-plane magnetic anisotropy in the sputtered thin films, aligning filed systems can be mounted in the cage housing (i.e. outside vacuum) in front of each magnetic target.

and total length, and the specific resistivity of wire material (e.g. copper, gold), R_{ac} is the resistance associated with the core loss (eddy currents and hysteresis) and skin effect, and R_d is the resistance associated with the dielectric losses caused by the capacitance of the coil turns with the wire acting as dielectric.

Typically, Q-factor is plotted against frequency (f), as shown in the inset of Fig. 2. For a given inductor size and core permeability, the Q-factor curves converge on the low frequency of the curve, where the losses are primarily determined by the DC resistance of the wires, and the frequency dependence of Q-factor is almost linear. By increasing the frequency, the Q-factor curves start to diverge and reach a peak ($Q = Q_{max}$) at a frequency where the copper and magnetic-core losses are equal. For a chosen core material the frequency at which this peak occurs is inversely proportional with the core size. Thus, for larger cores Q-factor reaches a maximum at lower frequency; moreover, larger cores have higher peak Q-factor than smaller cores. Beyond this region the magnetic-core losses prevail and Q-factor drops rapidly.

A high Q-factor is the inductor's most desired feature, and hence in the design and manufacturing process the series resistance (R) and distributed capacitance (C) should be as low as possible (see Fig. 2). Since, depending on the inductor design used (2D or 3D) one can increase Q by making the windings larger and using thicker metal layers (i.e. longer and thicker wires) at the expense of size, and using lower resistivity metals (e.g. Cu or Au instead of Al). Another method of improving Q-factor is to increase the resonance frequency of the inductor (see Fig. 2), which can be realised by increasing the spacing between the turns of the inductor (i.e. lower C) also at the expense of size, lowering the dielectric constant of the material between inductor's windings, using higher resistivity substrates and thick oxide layers between the substrate and metallic layers, and increasing the ferromagnetic resonance frequency of the magnetic-core material. The latter can be realised by selecting materials with high saturation magnetisation (M_s) and by increasing the anisotropy field (H_k) [4].

Fig. 4: Schematics of an integrated 3D inductor for on-chip RF applications, the magnetic core of which consists of a sputtered multilayer based on a low-loss soft magnetic material. The inset shows a cross-sectional transmission electron microscopy (TEM) analysis of a CoTaZr/Al_2O_3 soft magnetic multilayer sputtered on 8" Si/200nm-SiO_2 wafer. To lower the hysteresis and eddy current losses the ~80 nm thick CoTaZr layers are laminated with 4 nm thick Al_2O_3 dielectric interlayers.



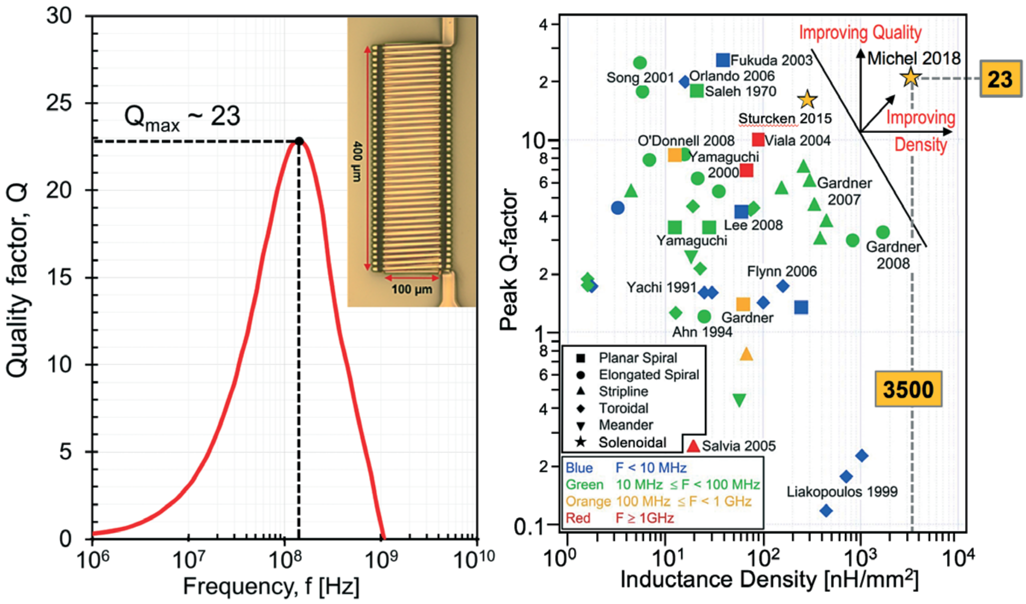


FIG. 5: a) Q-factor vs. frequency for a 100 µm x 400 µm magnetic-core solenoidal inductor depicted in the optical micrograph. b) Peak Q-factor vs. inductance density of integrated inductors on Si substrates from published on-chip inductor measurements (adapted from Reference [2]). The colors represent the frequency of the peak Q-factor.

Soft magnetic thin films at LLS EVO II

The vertical batch sputter system LLS EVO II (see Fig. 3) is a very versatile economical tool for depositing micrometer thick soft magnetic on substrates up to 200 x 230 mm. This system has several knobs for tuning the in-plane anisotropy of the sputtered soft magnetic layers. Thus, the performance of the magnetic cores can be tailored by appropriate choice of the magnetic material (saturation magnetization, electrical resistivity) and dielectric interlayer (dielectric constant) [5]. Further tailoring of the soft magnetic multilayer properties can be done by tuning the process parameters (e.g. pressure, power, deposition temperature, angular distribution) [6]. Last but not least, since in the LLS EVO II system the substrate cage rotates continuously during deposition, so that the substrates face different targets alternatively, each ferromagnetic sublayer in the multilayer stack may consist of a fine structure comprising alternating nanolayers with very sharp interfaces. Adjusting the thickness of these individual nanolayers by changing the cage rotation speed and the power applied to each cathode, allows to engineer new, composite ferromagnetic materials [4,7,8].

Integrated passive devices with record quality factor

Ultra-low profile integrated magnetic solenoid inductors and transformers were fabricated at CEA Leti on 200 mm high-resistivity silicon wafers with back-end-of-line (BEOL) process [9]. Bottom and top conductors were formed by electroplating with 10 µm thick copper, 5 µm line width, and 5 µm spacing between the lines. In order to have a good insulation and to reduce topology, the lines were embedded into a thick polymer. Then, the magnetic film consisting of a multilayer with alternating 80 nm thick CoZrTa amorphous soft magnetic layers and 4 nm thick Al_2O_3 dielectric interlayers were deposited by dynamic sputtering under a linear magnetic field using a LLS EVO II system (see Fig. 4). Finally, the wafers were grinded to reduce the silicon thickness down to 100 µm. By varying the core size, i.e. width (*l*) and length (*L*), and the winding pitch, a record inductance surface density of 3500 nH x mm2 in the 1 MHz to 3 GHz frequency range with a record peak *Q*-factor of 23 (see Fig. 5). This breakthrough sets a new benchmark of quality for cost-effective manufacturing of soft magnetic multilayers on silicon, and can therefore help manufacturers meet exacting standards for next generation thin film based integrated passive devices.

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