YOLE Group

Photonic integration in the AI era:
Navigating the next wave of optical interconnects

With AI clusters and hyperscale data centers driving bandwidth and energy efficiency demands, the photonic IC landscape is at a turning point. Yole Group analyzes the material platforms – SOI, LNOI, InP – and strategic trade-offs shaping the future of high-speed optical interconnects, from pluggable modules to co-packaged optics.

In the rapidly evolving optical interconnects market, demand for scalable, high-speed, energy-efficient modules is surging, fueled by AI clusters and hyperscale cloud data centers. Although CPO promises ultra-low power and high density, many network operators and system vendors continue to favor pluggable modules for their proven cost-effectiveness, easy front-panel access, and multivendor interoperability.

PICs are specialized chips that integrate various optical components, like lasers, modulators, and detectors, onto a single substrate, enabling the manipulation of light within a compact footprint. Silicon is one of the most widely used materials for photonic integration, especially in data center and telecom applications. Silicon photonics (linked to a SOI material platform) leverages CMOS-compatible processes, enabling large-scale, cost-effective manufacturing.

It's ideal for integration with other materials for functions like modulation and detection. Silicon photonics is often combined with InP material for hybrid or heterogeneously integrated light sources. Widely used hybrid integration will work for 100G/lane and should also work for 200G/lane, but beyond that, there are challenges that must be overcome.

To achieve 400 Gbps per lane and beyond, the industry is exploring deeper integration of exotic materials for modulators, detectors, and waveguides on SOI substrate. The heterogeneous integration of not only a III-V laser, but also exotic materials, adds complexity that lowers the yield and raises the cost of the PIC and delays the time to market. It is essential to design new PICs that meet the future bandwidth requirements and make them commercially viable.

Two strategic pathways: Higher speed per lane vs. Slow and wide optics

Higher speed per lane

Higher per-lane rates enable per-port Ethernet speeds of 3.2 Tbps (and beyond), while delivering roughly 20–30% power savings and a 50% reduction in laser count. Fewer lasers lower capex, simplify supply chains, and shrink operational expenses for cooling and power delivery. This strategy brings new opportunities for additional platforms into play. LNOI and InP are more straightforward solutions for future high-speed links due to intrinsic material properties.

LNOI benefits from excellent electro-optic modulation efficiency, ideal for ultra-high bandwidth applications targeting LPO, LRO, and coherent-lite pluggable optics. All TFLN/LNOI suppliers in this field have developed TFLN PICs which will compete with SOI in the same applications. However, it will be challenging at the beginning due to the high cost and limited mass production.
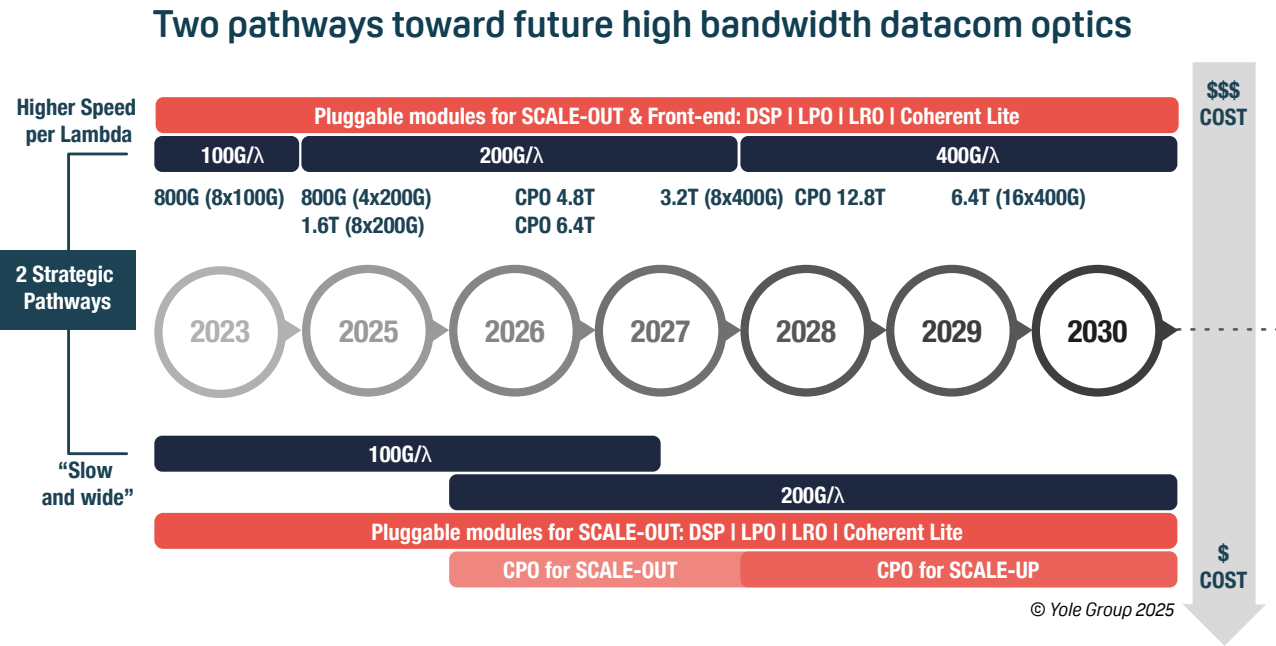
InP stands out for its ability to integrate active photonic components directly into the chip. This minimizes the need for complex assembly, though the technology currently incurs high costs and remains at a low production volume. InP could become a formidable competitor to SOI and LNOI by 2030, especially for coherent-lite applications.

Slow and wide optics

The yield of new materials integration on an SOI platform, as well as large-scale manufacturing of LNOI or InP platforms, may not meet cost expectations by 2028.
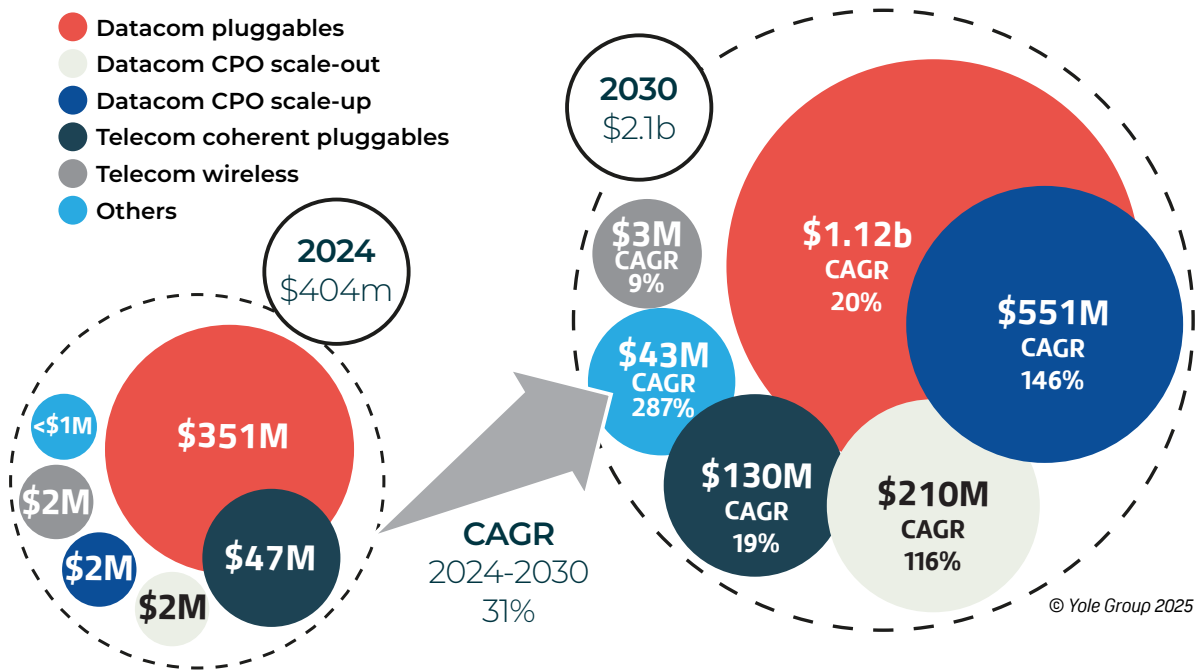
The "slow & wide" model unlocks simpler electronics, mature optical components, and high port densities. A high radix enables more lanes at lower speeds and cheaper modulators. As the integration of silicon photonics matures, expect the radix to climb even higher (16, 32, or more) to hit multi-terabit pluggable modules as well as CPO engines.

Slow and wide" optics hit high aggregate bandwidth by keeping each lane modest in speed while multiplying lanes across fibers or wavelengths, which eases analog design, improves signal integrity and margins, can lower per-lane power, reduce DSP complexity and latency, leverage mature, lower-cost components (especially for short reach), and often help yield and reliability. However, the approach pushes problems elsewhere: you need many more SerDes and fibers, which strains package pins, retimers, and co-packaging budgets and front-panel density. Slow and wide shines for short-reach intra-rack/row links and latency-sensitive AI/ML clusters using simple NRZ/PAM with light – ideal for CPO systems.

Two pathways toward future high bandwidth datacom optics

© Yole Group 2025

Related Yole Group's products
- *Optical Computing 2024*
- *Silicon Photonics 2025 - Focus on SOI, SiN, LNOI & InP Platforms*
- *CISCO - QDD-400G ZR-S Optical Transceiver Die Analysis*
- *Co-Packaged Optics for Data Centers 2025*
- *Optical Transceivers for Datacom and Telecom 2026*
- *Photonics Packaging 2026*
- *Quantum Technologies 2026*

Photonic integrated circuit market
Pics (dies) revenue growth forecast: by technology platform (2024 vs. 2030)

Legend:
- Datacom pluggables
- Datacom CPO scale-out
- Datacom CPO scale-up
- Telecom coherent pluggables
- Telecom wireless
- Others

2024 $404m
2030 $2.1b

CAGR 2024-2030 31%

© Yole Group 2025

Looking ahead

As data center operators demand ever higher bandwidth per watt and lower total cost of ownership, the battle among SOI (plus TFLN/BTO/polymer), LNOI, and InP platforms will intensify. Pluggable modules, whether IM-DD or coherent-lite, will continue evolving in speed, integration, and power efficiency. Meanwhile, CPO designs will need to demonstrate robust performance and ease of deployment before replacing pluggables in mainstream systems. The next five years will determine which material platform delivers the optimal balance of cost, power, and performance.

The silicon PIC (dies) market was worth $404M in 2024 and is forecast to grow to more than $2.1B in 2030 at a 31% CAGR2024-2030. This growth will be driven mainly by high-data-rate pluggable modules for increased fiber-optic network capacity. Additionally, projections of rapidly-growing training dataset sizes show that data will need to use light for scaling ML models using CPO in AI clusters.

About the Author

Martin Vallo, PhD, is Senior Technology & Market Analyst, Photonics at Yole Group. Martin specializes in optical communication and semiconductor lasers within the Photonics & Sensing activities at Yole Group. With 12 years' experience in semiconductor technology, Martin is currently involved in the development of technology & market products as well as the production of custom consulting projects.

Prior to his mission at Yole Group, Martin worked at CEA (Grenoble, France), where he focused on the epitaxial growth of InGaN/GaN core-shell nanowire LEDs by MOCVD and their characterization for highly flexible photonic devices.

Martin graduated from the Academy of Sciences, Institute of Electrical Engineering (Slovakia), with an engineering degree in III-nitride semiconductors.

Source: www.yolegroup.com