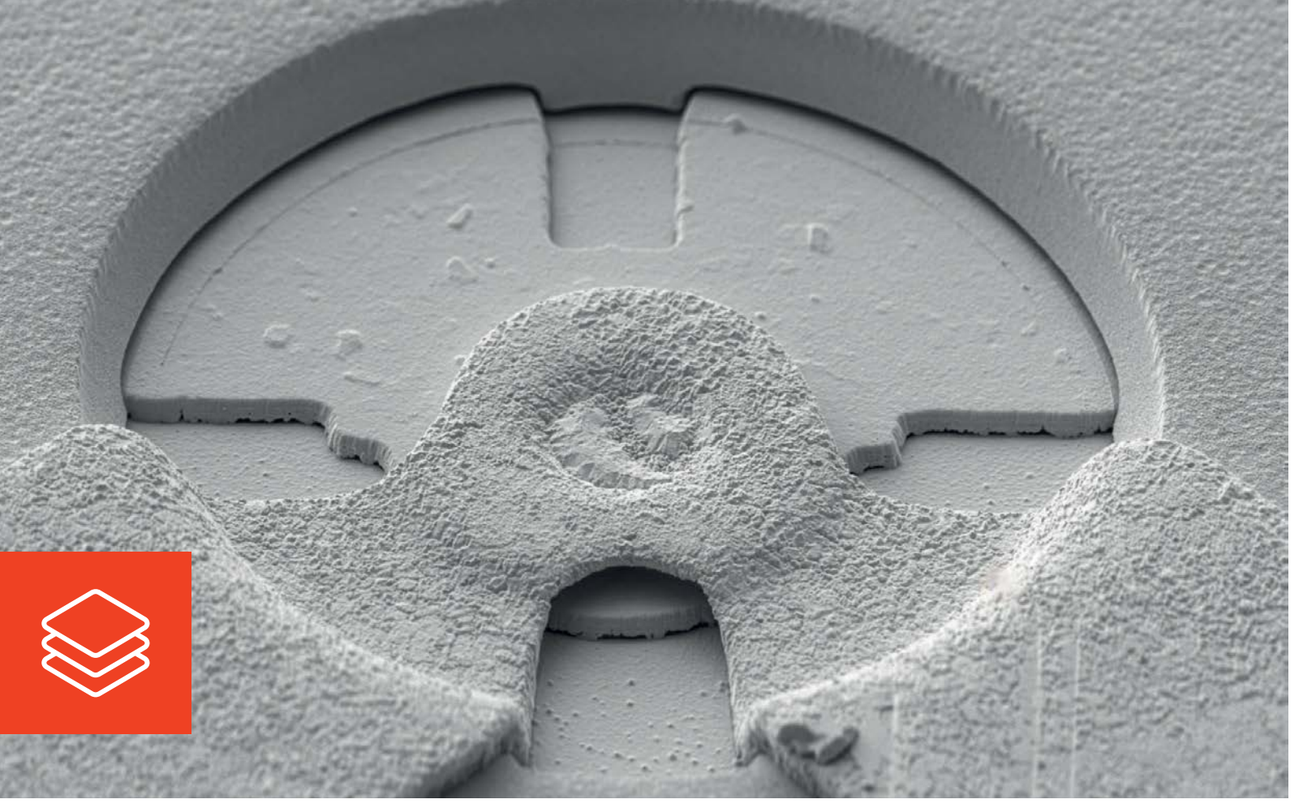

Development of a Highly Sensitive Test Vehicle for the Accurate Measurement of Seed Layer Contact Resistance in 2.0 µm-diameter Vias

Abstract

In the increasingly sophisticated semiconductor packaging landscape, multiple dies can be connected side-by-side on an interposer or stacked vertically to achieve shorter distances and higher interconnects density. These technologies allow the Heterogeneous Integration of chiplets with increased functionality, higher speed and better power efficiency. The high interconnects density and the concomitant shrinkage of the critical dimensions (e.g. RDL width/pitch and diameters of the vertical interconnections), increase exponentially the importance of the contact resistance between metal interfaces. In wafer-level packaging, interconnects are commonly manufactured by sputter deposition of a seed layer followed by Cu electroplating. The main challenge, prior PVD, is the elimination of the native oxide present on the exposed metal contacts, coupled with the presence of organic load released by the polymer dielectrics widely used in WLP (e.g. PI and PBO) that contaminates the process chambers of the PVD platform.

This work presents an improved wafer-level manufacturing process for fabricating Kelvin resistors based on Al/Ti/Cu metallization and via diameter ranging from 2.0 µm up to 20.0 µm. Experimental R_c data have shown that the sensitivity of the fabricated structures, in regard of the chamber conditions, is inversely proportional to the contact area. A test run of 25 wafers processed at a throughput of 55 wafers/hour on the HEXAGON has revealed a constant R_c on 10.0 and 20.0 µm via structures, but instead a significant excursion on the smaller vias. For example, 2.0 µm via structures exhibited R_c = 36.5 mΩ on wafer#1 and R_c = 44 mΩ on wafer#25. This corresponds to a 20% increase within lot. In conclusion, the fabricated Kelvin resistors are very suitable test vehicles to be used for benchmarking PVD seed layer processes and to establish optimum conditions ensuring high yield and a constant wafer-to-wafer quality in next-generation high-density interconnects WLP applications.

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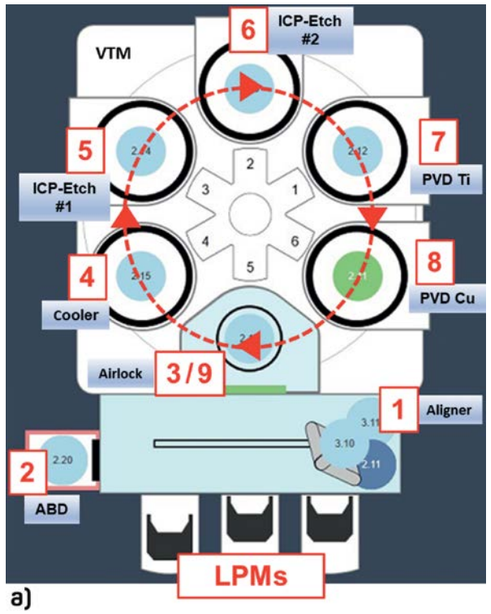
Introduction

The increasing demand for devices with higher speed and increased power efficiency, fueled by High-Performance Computing (HPC) and Artificial Intelligence (AI), is driving tremendous innovations in the electronics industry, both in frontend-of-line (FEOL), but even more in the field of advanced packaging [1]. TSMC's Chip-on-Wafer-on-Substrate (CoWoS) [2,3] and ASE's Fan-Out-Chip-on-Substrate (FOCoS) [4,5] are two examples of cutting-edge wafer-level packaging (WLP) technologies. Both combine multi-level fine-pitch redistribution layers (RDL) with shorter interconnect lengths and micro-bumps to enhance signal speed and power efficiency in 2.5D and 3D architectures. These technologies offer the advantage of a larger package size and more I/O connections per unit area. In addition, horizontal 2.5D and 3D stacking configurations of components enable the Heterogenous Integration of various processor and memory modules layer by layer, e.g. logic System-on-Chip (SoC) and High-bandwidth Memories (HBM) on the same IC platform [6,7].

Latest developments in advanced WLP applications often require RDL technologies with critical dimensions below 10 micrometers [8,9]. Therefore, a tight control of the contact resistance (R_c) is becoming increasingly important in high-volume manufacturing (HVM) to ensure high yield and a constant wafer-to-wafer quality. The smaller scaling of the interconnects is coupled with the presence of high loads of volatile contaminants released by the organic passivations widely used in WLP. The latter are typically spin-coated films of Polyimide (PI) or Polybenzoxaxole (PBO). State-of-the-art packaging platforms require the implementation of advanced strategies to mitigate the impact of hydrocarbon species and oxide contamination on the metal interfaces to avoid an adverse impact on R_c [10-13].

This work presents a wafer-level manufacturing process for the fabrication of Kelvin resistors based on the interface between a bottom Al electrode and an upper Ti/Cu metallization. A 5.0 µm-thick PBO passivation is present on the wafer, separating the two metallization levels, for mimicking the organic load of real WLP products. Various Kelvin structures with via diameter ranging from 2.0 to 20.0 µm have been designed. The smaller the via size, the higher the sensitivity of the structure in regard of process parameters and chamber conditions. The fabricated Kelvin resistors are suitable test vehicles to be used for monitoring the performance of the PVD process based on different throughput and conditioning frequency. The goal is to establish a set of optimum conditions that allow to keep low and stable R_c for a given via size at the highest throughput.

In a multi-level interconnects scheme, such as CoWoS and FOCoS, the PVD stack is present at numerous interfaces: (1) between the chip I/O's (i.e. Aluminum pads), and the first RDL, (2) between multi-level RDLs and (3) between the uppermost RDL and the under-bump metallization (UBM). The quality of these interfaces plays a fundamental role in the overall electrical device performance in terms of power consumption and signal integrity.



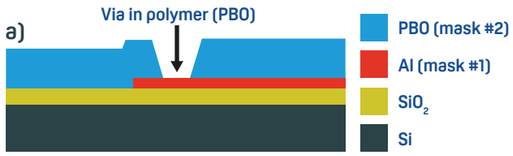
LPMs	
1	Aligner
2	Atm. Batch Degas

Figure 1:
a) State-of-the-art 300 mm HEXAGON used in high-volume manufacturing of wafer-level packaging,
b) Corresponding process flow that includes wafer pre-treatment steps and the deposition of adhesion and seed layers.

b)

In WLP, the adhesion/seed film stack is commonly deposited in state-of-the-art Cluster-type or Indexer-type multi-chamber PVD systems [14]. The wafer is pre-treated prior to the sputter deposition of the metal stack. First, degas is applied to drive out moisture from the organic passivation. This is followed by ICP sputter etch in Ar plasma to eliminate the native oxide from the exposed metal contacts. To ensure a low and stable R_c, especially at high throughputs, it is of utmost importance to mitigate the risk of re-contamination of the cleaned contacts by the volatile byproducts generated during the non-selective sputter etching of the wafer surface. The process strategy implemented on the Indexer platform has demonstrated best R_c control at the highest throughput achieved in HVM (Figure 1) [15]. The periodic conditioning of the ICP sputter etch chambers by "Aluminum pasting" is an integral part of the state-of-the-art process strategy implemented in the Indexer platform [10]. Pasting is an interruptive process that consists in the sputter etching of dedicated Al coated wafers, or bulk Al plates.

Keywords—Kelvin resistor, R_c, ICP sputter etch, PVD, seed layer, indexer, throughput



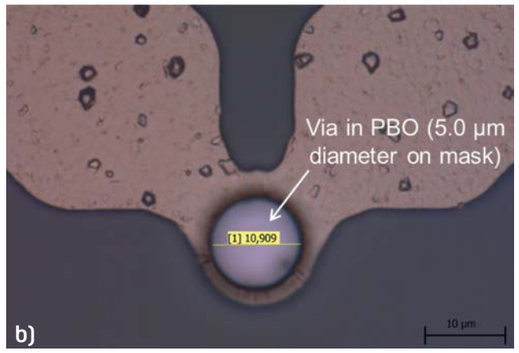
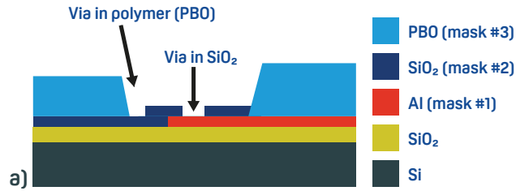


Figure 2: Fabrication process "Generation 1": a) schematic via cross-section before PVD seed layer, and b) top view of a via through PBO with 5.0 µm nominal diameter on mask. The measured opening is 10.9 µm.



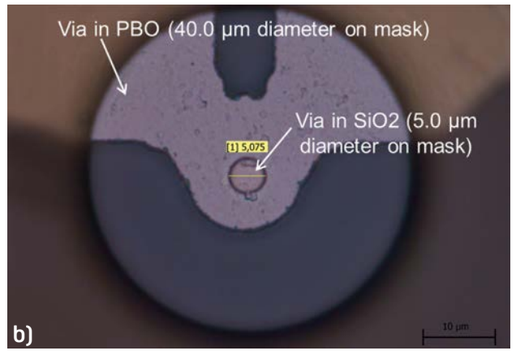


Figure 3: Fabrication process "Generation 2": a) schematic via cross-section before PVD seed layer, and b) top view of a 5.0 µm-diameter via through SiO_2 surrounded by a 40.0 µm-diameter via through PBO.

Al is a well-suited material for the pasting process due to its high chemical affinity towards volatile species, in particular oxygen, and its 50% higher sputtering rate in Ar plasma compared to SiO_2. Two main benefits are associated to the Al pasting process. These are the gettering effect on volatile contaminants, which can be measured by the rapid drop in the chamber base pressure, and the binding of solid residues onto the shields, that mitigates or delays the formation of particles. Generally, the first wafer processed after Al pasting benefits from best chamber conditions.

Experimental Method
Fabrication of Kelvin Resistors

In this work, Kelvin resistors are built on 300-mm Si wafers passivated with thermally grown oxide. As a first step, 1.0 µm-thick Al is sputter-deposited and patterned by reactive ion etching (RIE) to form the bottom electrode. Next a 5.0 µm-thick PBO passivation (HD-8820 from HD MicroSystems) is spin-coated and cured according to the temperature recommended by the supplier. A descum process in O2 plasma is carried out to remove PBO residues in the vias after the patterning by UV photolithography. In an earlier stage of our research, the mask-set referred as "Generation 1" was designed to include test structures with various via diameters ranging from 5.0 µm up to 30.0 µm. The fabricated vias systematically exhibited a tapered shape where the top opening exceeded the nominal diameter on the mask as shown in Figure 2a and 2b. A new mask-set has been designed and the corresponding fabrication process "Generation 2" has been established to overcome the resolution limitations of PBO photolithography in vias of aspect ratio (AR) = 1:1 and higher. The smaller the via diameter, the more sensitive the structure becomes in regards of the process parameters and chamber conditions.

Consequently, these new test vehicles allow to expand the R_c study towards more advanced interconnection schemes. To effectively achieve contact areas below 5.0 µm, a first set of vias is patterned by RIE into a 400 nm-thick PECVD SiO_2 film protecting the Al electrode (Figure 3a). Several design variations of round vias with diameter ranging from 2.0 µm up to 20.0 µm are present on the mask-set. The formation of SiO_2 vias is followed by PBO photolithography to open larger vias surrounding the previously formed ones. Beside the small contacts to the subjacent Al electrode, the PBO passivation layer on the wafer serves to mimic the organic load present on real WLP products. Figure 3b is a top view showing the two concentric vias: i.e. the 40.0 µm-diameter via in the PBO surrounding a 5.0 µm via patterned in the SiO_2 film.

Both in "Generation 1" and "Generation 2", after the formation of vias, the fabrication flow continues with the PVD seed layer process carried out on the Indexer platform (Figure 1). Here, the physical processes taking place include degassing at 120°C for 30 minutes, ICP sputter etch to remove a thickness of 30 nm equivalent to SiO_2, and finally, the sequential deposition of 100 nm of Ti and 200 nm of Cu. The downstream process continues with the formation of photoresist (PR) molds for the subsequent electroplating of a 3.0 µm-thick Cu film to reinforce the PVD seed layer. With an additional PR mask, Ni/Au electroplating is performed selectively on the four probing pads to provide a more reliable contact during probing. After electroplating, the PR layers are stripped and the Ti/Cu PVD films are wet-etched. As a last step, O2 plasma ashing is performed to remove any residues of seed layer left on the PBO surface that could potentially lead to shortcuts during the electrical characterization. The 25-wafers lot was processed on the Indexer system with the process-of-records resulting in a steady-state throughput of 55 wafers/hour.

There are differences in the number of total design variations and the base cell dimensions between mask-sets "Generation 1" and "Generation 2", but these are not relevant for the general description of the layout of the fabricated test structures. A 300-mm "Generation 1" test wafer (Figure 4a) contains approximately 750 base cells, each of these is constituted by an array of 11 x 11 = 121 structures (Figure 4b). Design variations include different via size and other parameters, e.g. the overlap width and access conductor width, that were investigated elsewhere [16]. Figure 4c is an enlargement of the base cell showing the layout of the fabricated 4-terminals Kelvin resistors. The size of the probing pads is ≈200 µm by ≈200 µm. Figure 4d is a zoomed view of the overlap area between the bottom Al electrode and Ti/Cu metallization with a 10.0 µm-diameter via in the center. Figure 4e shows a FIB cross-section of the contact area, revealing the tapered shape of the via formed in the PBO layer.

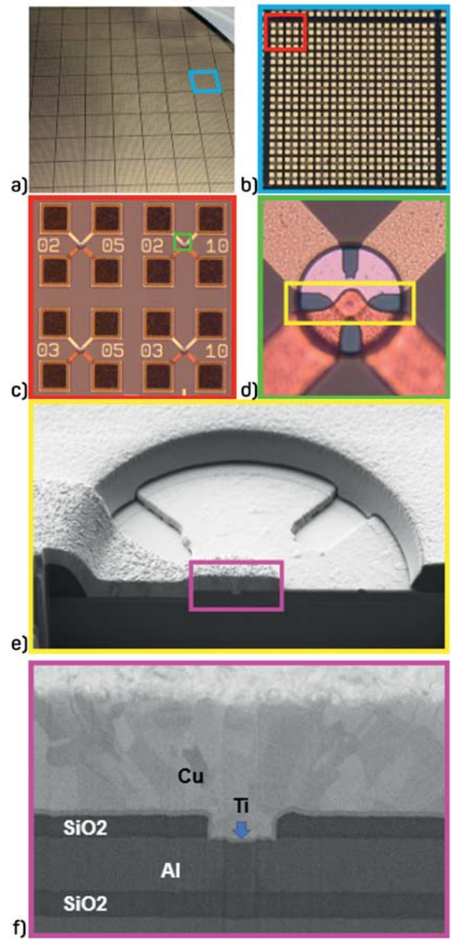


Figure 4: a) Fabricated 300 mm test wafer of "Generation 2", b) base cell containing an array of 11 x 11 Kelvin structures, c) example of Kelvin resistors layout, d) magnification of the contact area, e) FIB cross-section of the contact area of a 2.0 um-diameter via in SiO_2, and f) close-up of the interface between the underlying Al and the upper Ti/Cu metallization.

Electrical Characterization

The device characterization is performed at the wafer-scale using a vertical probe card. Four-points resistance measurement is conducted by forcing a current of 50.0 mA from terminal A to C, according to the sketch represented in Figure 5, and simultaneously measuring the potential difference between the opposite terminals B and D. The resistance of the Kelvin structure is calculated as the ratio of voltage divided by current: $R_K = V_{BD} / I$. In this study, R_K is considered as the contact resistance, R_c. However, an equivalent model has shown that R_K not only contains the R_c term, but also a geometrical factor, R_{GEOM} that accounts for 2-D current flow effects around the contact area [17]. Experimental data have shown that R_K increases when the overlap formed between the bottom and the upper metallization around the via becomes wider [16].

Contact Resistance Benchmark

The procedure to evaluate the stability of R_c in HVM-like conditions consists in placing electrical test wafers in slots #1, #13 and #25 of a 25-wafers lot, while the remaining slots are populated with PBO-coated dummies that mimic the outgassing load of real product wafers (Figure 6). In this study, the conditioning of the ICP sputter etch chambers by Al pasting is performed before the first wafer of the test lot.

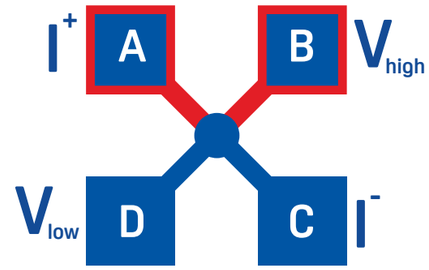


Figure. 5: Electrical characterization of 4-terminals Kelvin resistors.

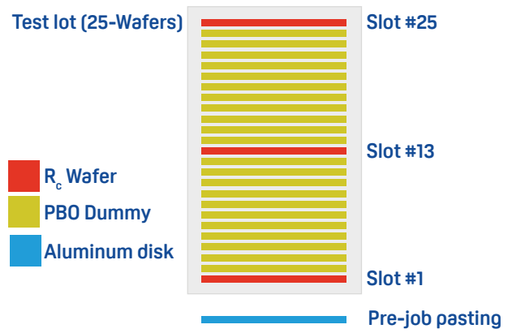


Figure 6: Procedure for the characterization of R_c stability within a 25-wafers lot. In this study, the ICP sputter etch chambers of HEXAGON are conditioned by Aluminum pasting prior processing the test lot.

Results

Figure 7a displays the R_c performance vs. via size obtained on structures of "Generation 2". As expected, R_c exhibits an increasing trend with the reduction of the via size. Structures with via diameter 20.0 µm show a R_c in the order of 3.0 mΩ, while structures with via diameter of 10.0 µm result in a R_c value of approximately 6.5 mΩ. In both cases, R_c remains constant within the lot. In contrast, a significant R_c trend-up can be observed on the smaller structures with via diameter ≤5.0 µm. The baseline of wafer#1 for the structures of via size 5.0 µm is ≈13 mΩ. This increases by 11% on wafer#25. The baseline of wafer#1 for via size 3.0 µm is ≈22 mΩ. Here, the increase within lot is 19%. Finally, the 2.0 µm via structures of wafer#1 exhibit a R_c of ≈36.5 mΩ and ≈44 mΩ on wafer#25, corresponding to an increase of 20%. Beside the geometrical factor predicting higher R_c for structures with smaller vias, the latter also exhibit a higher trend-up within the lot. Clearly, the accumulated contamination in the chamber during continuous wafer run has a more detrimental effect on the vias ≤5.0 µm.

Ho et al. reported R_c values of ≈20.0 mΩ measured on Kelvin resistors built with Cu/Ti/Cu metallization and a 2.4 µm-diameter via in 5.0 µm-thick polymer [9]. Our previous research has also demonstrated that the contact resistance measured on Cu/Ti/Cu interfaces is generally lower than the value measured on Al/Ti/Cu structures with same geometry [18].

Figure 7b compares side-by-side the R_c datasets of Kelvin resistors of "Generation 2" and "Generation 1" with 5.0 µm vias. Structures of "Generation 1" exhibit a lower R_c baseline and a larger data spread compared to "Generation 2". The inspection of the fabricated structures of "Generation 1" has revealed that the vias patterned in 5.0 µm-thick PBO have a tapered shape with a 50% enlargement of the opening at the top compared to the mask design (see Figure 2b).

This enlargement is caused by limitations of the photolithography resolution and very likely also by the step of plasma ashing after photolithography. The larger experimental spread may also indicate that the contact area is not constant over the entire wafer surface. On the other hand, structures of "Generation 2" reveal via openings in the SiO_2 passivation that are identical to the mask design (see Figure 3b). A narrower R_c spread is desirable as it allows for a more reliable benchmark between different process conditions.

Conclusion

A novel wafer-level manufacturing process has been developed to build Kelvin resistors with miniaturized via sizes. The approach consists in first patterning a via into a 400 nm-thick SiO_2 passivation covering a bottom Al electrode. This is followed by the patterning of a larger via surrounding the first one, in a 5.0 µm-thick spin-coated PBO passivation. The fabrication process is completed by the patterning of a Ti/Cu upper metallization. To our best knowledge, this work reports for the first time R_c data measured on Kelvin resistors with via size as small as 2.0 µm on Al/Ti/Cu contacts.

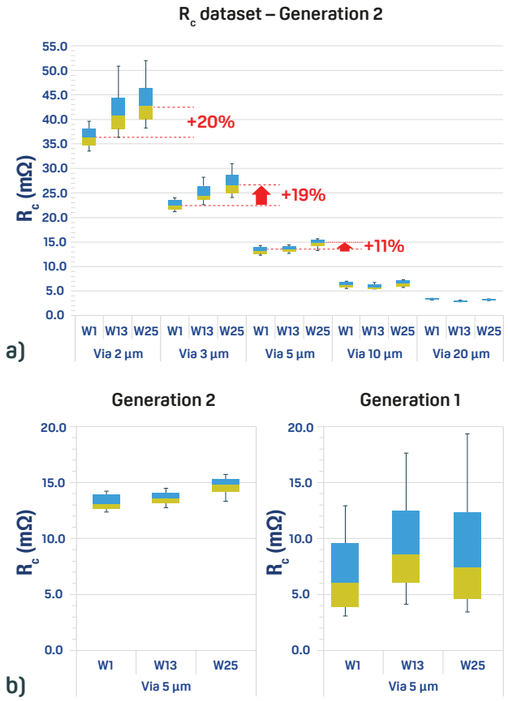


Figure. 7: a) R_c performance vs. via diameter and wafer position for Kelvin resistors fabricated with the improved process "Generation 2", and b) comparison of R_c obtained on 5.0 µm via structures of "Generation 1" and "Generation 2".

Experimental data has demonstrated that the process-of-records executed on the HEXAGON at a throughput of 55 wafers/hour and Al pasting performed before the test lot, delivers low and stable contact resistance in structures with via diameters of 10.0 and 20.0 µm.

In contrast, an excursion of R_c within lot can be observed on structures with via size ≤5.0 µm. This can be attributed to the accumulated load of volatile contaminants especially in the ICP etch chambers during continuous run at throughput of 55 wafers/hour and indicates excellent sensitivity of Kelvin resistors of "Generation 2" in regard of the process environment. Therefore, these test vehicles are suitable for optimizing PVD seed layer process conditions in HVM of current and next-generation high-density interconnects WLP applications.

Future work will include the optimization of the Aluminum pasting frequency allowing to keep R_c stable within lot, especially at peak throughputs above 90 wafers/hour that can be reached on the HEXAGON.

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