
89
20
WED
3457
STEPS
405 cal
28 mins
135%
6 hrs
THU
28
3457
THU 28
3457
steps

KEY CHALLENGES IN FAN-OUT PACKAGING TECHNOLOGIES

Mr. Byung-Lyul Park, VP Samsung Electro-Mechanics Co. Ltd. talks about working with Evatec to solve challenges in Fan-out packaging technologies for successful production of Samsung's GALAXY watch.

Taking the challenge

It is a well-known that the famous "Moore's Law" is reaching its limit due to physical challenges. In the early 70's, the Intel 4004 or 8008 processors had less than 5'000 transistors on the chip (figure 1). The latest IC chip from Samsung is a one Terabyte 3D-stacked VNAND flash memory chip containing 2 trillion MOSFETs (4 bits per transistor). These high-density packages also come with an increasing number of I/O's per chip which leads to a limitation of bump assembly, mainly bump pitch distance and size.

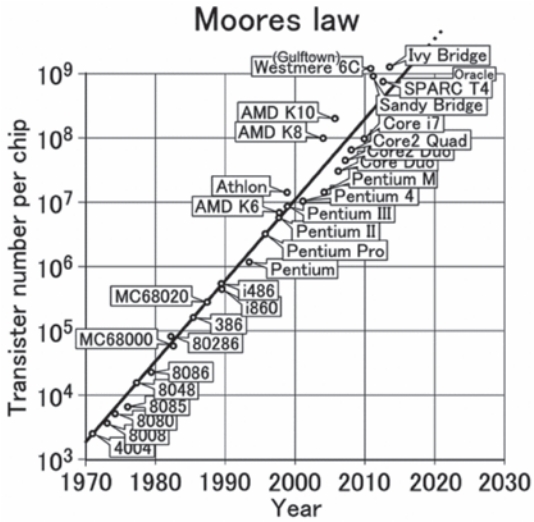

Figure 1. Moores Law

One solution to overcome this limitation is to Fan-out into the outer, additional area of the chip. To achieve this in mobile applications, we go from a Package-on-Package (PoP) solution, e.g. DRAM on Application Processer (AP) to a Fan-out PoP solution. This provides us with a thinner and therefore "cooler" solution with increased I/O density and in a next step aims for Fan-out System in Package (SiP) followed by the latest evolution into Fan-out SiP including integrated Sensors, AP, MCU's and passives into one package.

Packaging is a very cost driven and sensitive market, and our decision to move from wafer Level Fan-out to panel level Fan-out was with a clear goal of creating additional value both internally and externally for our customers. It is an example of our strategy in action, "competitiveness by innovation and a change in mindset" (see figure 6).

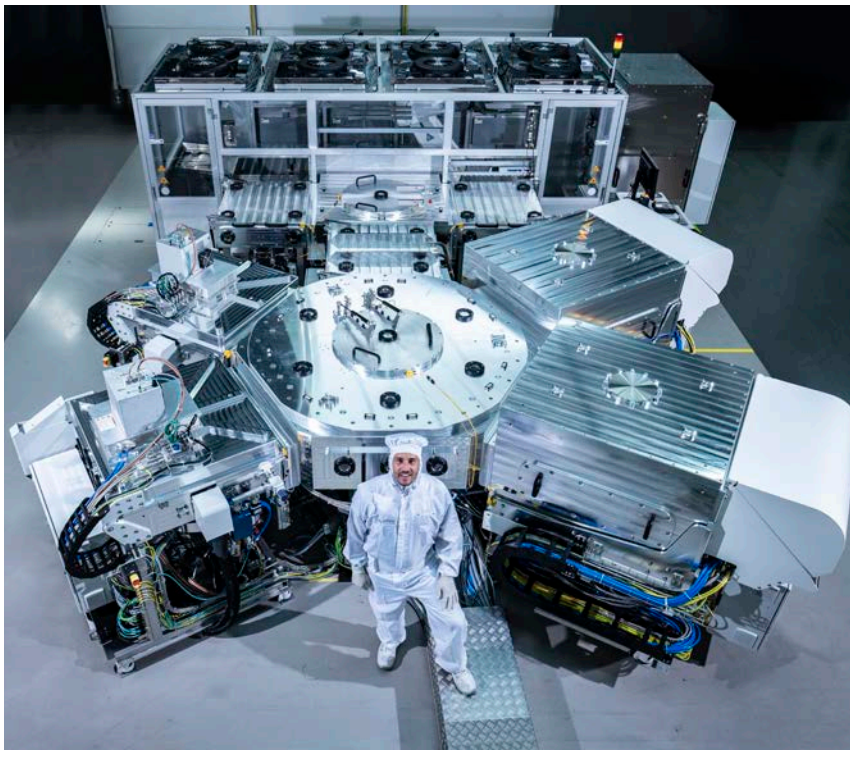

Figure 2. CLUSTERLINE® 600 - Evatec's second generation panel processing tool

Key success factors

With Evatec and their solution for a panel level sputtering tool we found a strong and reliable partner to help us solve the 3 main challenges we needed to address.

1. Warpage of the substrate
2. Fine pitch RDL
3. Process reliability

In the first key challenge, we had to deal with warpage, caused by a wide range of coefficient of thermal expansion (CTE), various thickness of the carriers used in production and several other challenges including the mold compound itself. With its long history in handling thin and warped substrates Evatec's CLUSTERLINE® panel processing tool provided exactly the solution Semco needed for reliable handling of warped panels in a production environment.

Figure 3. Rotating cathodes in PVD chamber

Fine pitch RDL with via sizes in the range of 20µm and a Line/Space (L/S) down to 5/5µm is not only a challenge for stepper tools or electroless copper plating tools but also for sputter tools. This is linked to the need for good thickness uniformity over the panel for titanium and copper layers, good side wall coverage in the pad vias, no residuals in the pads to provide outstanding bump resistance plus void-free interfaces between metal pad and RDL.

This second challenge could also be addressed by Evatec's CLUSTERLINE® panel tool with specially developed capabilities. These included batch degassing, conductive coupled plasma etching (CCP) and a unique sputtering approach with rotating cathodes (figure 3) allowing panels to be processed in static mode in the etch and deposition chamber. This reduced the risk of creating particles to a minimum, another crucial factor in fine Pitch RDL especially considering our roadmap going down to L/S of 2/2µm (figure 4).

Finally, the third challenge of process reliability was probably one of the most important to master. As with warpage and fine Pitch RDL, Evatec was once more able to support us with a solution which passed our internal reliability tests including Highly Accelerated Stress Tests (HAST), thermal cycling, high temperature storage tests over 1000 hours @ 150°C and drop testing.

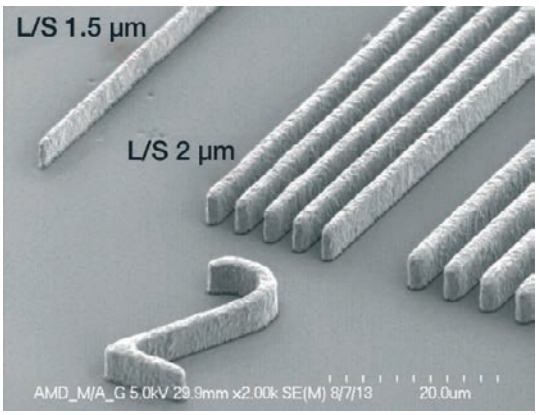

Figure 4. L/S 2/2/µm and L/S 1.5/1.5µm

Achieving success

Our efforts have been rewarded with the world's first FOPOP in high volume manufacturing supporting production of the Samsung GALAXY Watch (figure 5). The package size could be reduced to 76mm², which is around 65% of the previous package size, the RDL L/S at 7/8µm with a joint pitch to memory of 150µm.

Partnership is key

Figure 5. Samsung GALAXY Watch

We are glad to have Evatec as our partner supporting us in our strategy with the right solution for our Fan-out packaging technology on panel level for next generation business opportunities in the electronics parts industry. We look forward to further co-work with Evatec in exciting new challenges to come.

About Semco

SAMSUNG ELECTRO-MECHANICS

Samsung Electro-Mechanics (Semco), aims to be a world leader in the development in boards, chip parts, camera modules and communication modules.

Established almost a century ago in Korea, Semco fosters next-generation business opportunities to make its next leap as the leader in the electronics parts industry. The company sells over 80% of its products overseas.

The Chinese Hanja root word of Samsung Electro-Mechanics' Korean name "삼성전기" (Samsung Jeon-Gi) is 三星電機 with Jeon (전, 電, Diàn in Chinese), which means electricity, and Gi (기, 機, Jī), which means machine. The full name of Samsung Electro-Mechanics in English is Samsung Electromechanics, referring again to electronics and machinery.

Mission

To contribute to human society by providing top quality products and services based on talent and technology.

Vision

To be the best electronic parts company in the world.

Strategy

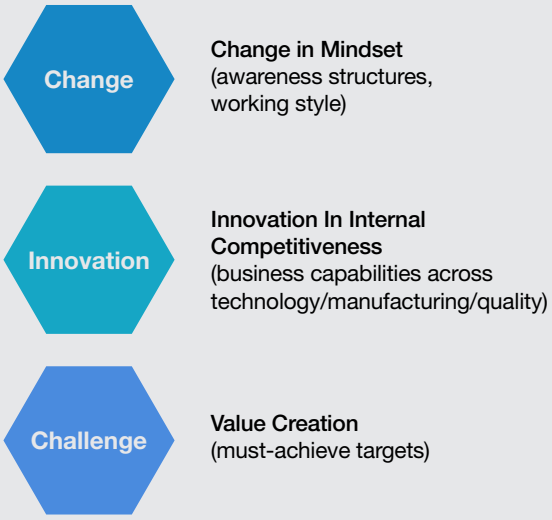

Figure 6. Change, Innovation & Challenge – key pillars of Semco Strategy

Read more...

Read more about Semco's activities in Fan-out level packaging when Santosh Kumar, from Yole, interviewed **Richard Bae**, Vice President, Head of Corporate Strategy & Planning Team, Samsung Electromechanics (SEMCO) (RBA).

www.systemplus.fr/Fan-out-panel-level-packaging-foplp-samsung-is-playing-a-strategic-game/

Cover Images and figures 1, 4 & 5 courtesy of SEMCO