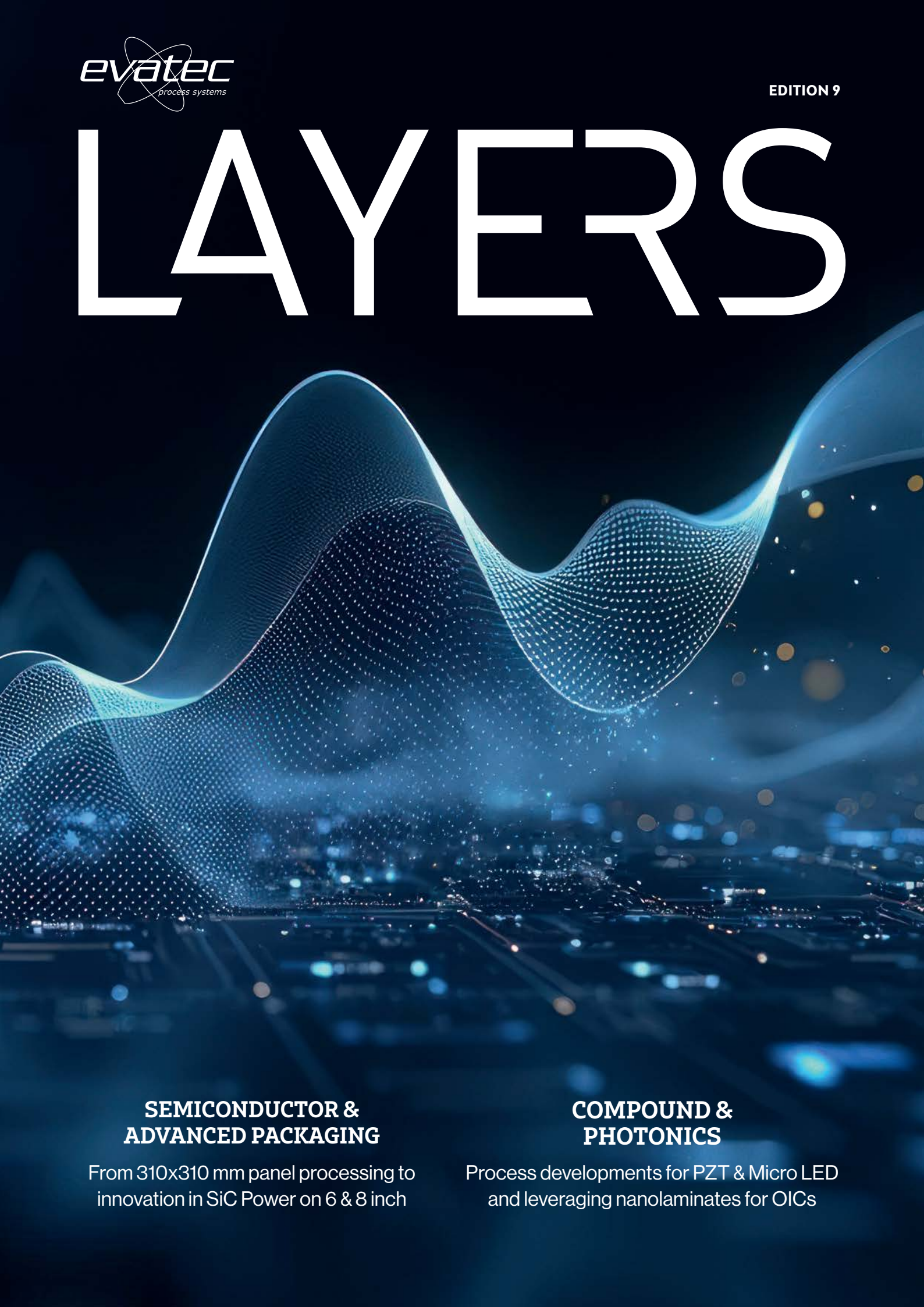
evatec process systems

EDITION 9

LAYERS



SEMICONDUCTOR & ADVANCED PACKAGING

From 310x310 mm panel processing to innovation in SiC Power on 6 & 8 inch

COMPOUND & PHOTONICS

Process developments for PZT & Micro LED and leveraging nanolaminates for OICs

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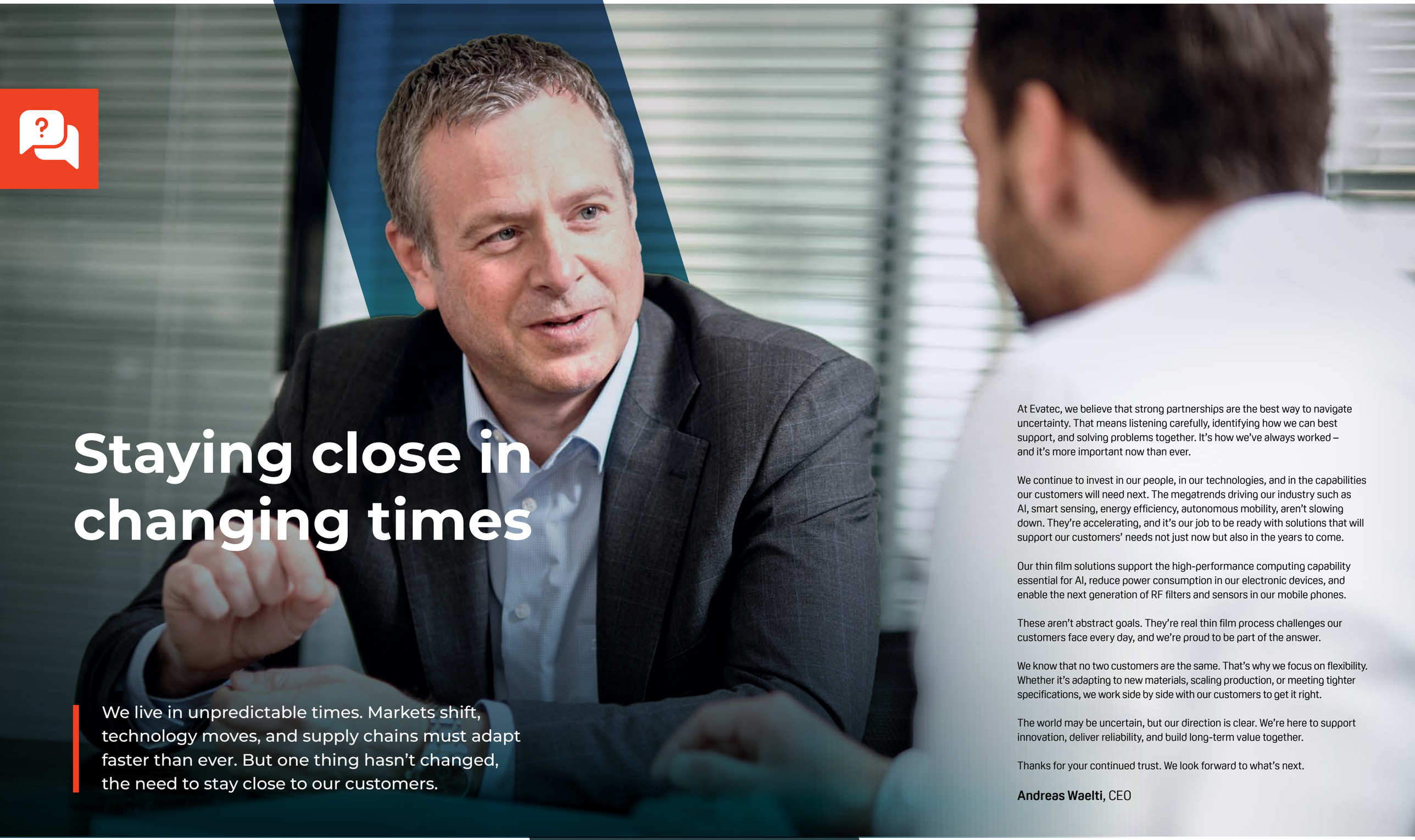

Staying close in changing times

We live in unpredictable times. Markets shift, technology moves, and supply chains must adapt faster than ever. But one thing hasn't changed, the need to stay close to our customers.

At Evatec, we believe that strong partnerships are the best way to navigate uncertainty. That means listening carefully, identifying how we can best support, and solving problems together. It's how we've always worked – and it's more important now than ever.

We continue to invest in our people, in our technologies, and in the capabilities our customers will need next. The megatrends driving our industry such as AI, smart sensing, energy efficiency, autonomous mobility, aren't slowing down. They're accelerating, and it's our job to be ready with solutions that will support our customers' needs not just now but also in the years to come.

Our thin film solutions support the high-performance computing capability essential for AI, reduce power consumption in our electronic devices, and enable the next generation of RF filters and sensors in our mobile phones.

These aren't abstract goals. They're real thin film process challenges our customers face every day, and we're proud to be part of the answer.

We know that no two customers are the same. That's why we focus on flexibility. Whether it's adapting to new materials, scaling production, or meeting tighter specifications, we work side by side with our customers to get it right.

The world may be uncertain, but our direction is clear. We're here to support innovation, deliver reliability, and build long-term value together.

Thanks for your continued trust. We look forward to what's next.

Andreas Waelti, CEO

CORPORATE & TECHNOLOGY HOTSPOT

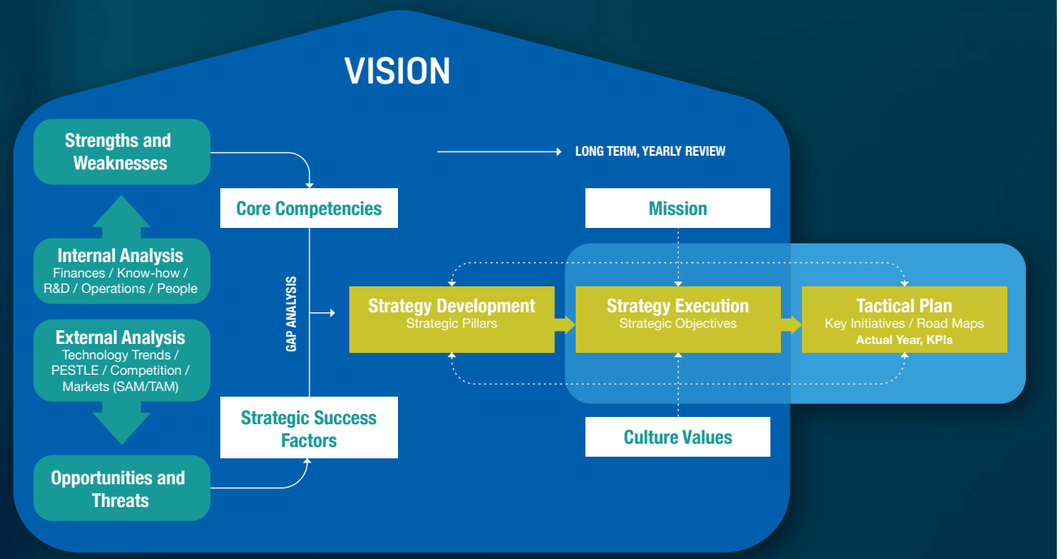

Figure 1: Evatec's Strategy Process

Strategy in Action

Senior Strategic Marketing Manager, **Maurus Tschirky**, introduces and illustrates the Evatec strategy process in action through some typical examples. It drives our activities in the medium and long term whilst still maintaining short-term flexibility, allowing us to adapt to challenges and opportunities in the market.

The process itself – in a nutshell

When asked about a contribution relating to Strategic Marketing and Business Development, the first dilemma was how to put down something of broad interest to readers of LAYERS without going into endless process details or sharing strategic plans intended for internal consumption only... but hey, aren't we here for making possible what seems to be hard at first sight?

So, rather than elaborating the whole Strategy Process per se and losing the reader's attention within 10 seconds, my focus here is more on reporting its impact. I intentionally don't touch the many workshops and methodology applied but hope that the single sketch about the Strategy execution in Figure 1 explains the essential parts of our process.

I then showcase two examples to illustrate the outcome of a lot of work carried out behind the scenes.

It starts with the company vision. Then as in any strategy process, there follows a thorough analysis of the status quo both internally and externally. The outcome generally answers the questions about what we ARE able to do in comparison to what we NEED to be able to do. The identified gaps represent the playing field for the Strategy Development.

The general directions are defined here, with the clear purpose of serving as guidelines for the detailed items within the Tactical Plan. Any activity therein must follow the general direction and contribute to the overall goals. We are aiming to create an environment that is agile and flexible to adapt to the market's needs. "Strategic Marketing and Business Development" very much go together.

While the internal analysis is often rather straight forward, the external factors appear ever more complex – most prominently represented by the currently unpredictable and erratic geo-political turmoil. Make no mistake, the SEMI Industry is probably the most globalized eco-system you can find. Without global contribution, participation and free trade, this industry would not be where it is today.

At the same time, the market creates certain positions of strength and power, clearly resulting in dependencies. The widespread use of thin film technology gives rise to a heightened awareness of the strategic opportunities of being able to tap into the supply of semiconductor devices. However, localization, various 'Chip Acts', countless regulations and restrictions might even pave the way for the establishment of competing spheres.

The situation is consequently very complex, and things can also happen outside our range of influence, with either detrimental or beneficial effects.

Continuously assessing the latest developments is therefore essential and that's exactly what we do in regular reviews. What therefore might come across as straight forward and utterly logical is, in fact, much more complicated than at first glance. Human factors and company culture both have a huge influence on the outcome of this highly dynamic process which takes place under the umbrella of the company vision, values and management principles.

Our process recognizes both the need to remain agile for the short-term, whilst being persistent on activities for the mid- and long-term. The big picture lasts longer and enables major developments and programmes over several years, whereas the Tactical Plan defines the Initiatives and KPIs for the actual year. But let's leave the theory behind and introduce two real examples of our Strategy Execution:

Market Segments	MEMS	Wireless	Power	WLO
Materials	AlN, AlScN, PZT, KNN	AlN, AlScN, SiGe, $LiNbO_3$, ($LiTaO_3$)	GaN	$LiNbO_3$, $BaTiO_3$
Properties		Highest crystallinity, quasi-epitaxy for all materials		
Seeding	t.b.d.	t.b.d.	Hot AlN buffer	$SrTiO_3$ for BTO
Material Class		'Functional Ceramics' (Wurtzites, Perovskites, ...)		
Hardware Features		Temperature, Low Energy Impact, Seeding		

Figure 2: Evatec breakdown of requirements, hardware and processes

1. An EPIC* story out of the Internal Analysis

We start with an important activity that has its roots in the deep-dive analysis of our core competencies – the internal analysis. A growing number of requests and needs from various market segments appeared to reveal certain similarities. From Gallium Nitride (GaN) in Optoelectronics and Power Devices, to Lithium Niobate (LNO) and Aluminium (Scandium) Nitride (Al(Sc)N) for Wireless and Photonics, Barium Titanate (BTO) for Photonics, we recognized the general need for highest crystallinity of a somehow related class of materials (Figure 2).

Luckily, we have dealt with some of those materials for two decades already. Piezoelectric effects have been at the heart of our success in MEMS and Wireless applications over years, with ferroelectricity now opening new applications and electrooptic properties gaining momentum due to the growing importance of Photonics in the industry. These properties and characteristics, often called multiferroics, are at the very heart of functional materials with regards to transducing one physical quantity into another one.

Many of those materials require particular hardware and process control features in our systems to achieve the specified properties. That's what we have been developing so far and continue to develop as part of our long-term strategy.

Footnote: EPIC is an acronym combining the words Epitaxy and Photonic Integrated Circuits.

2. External view allows for reaching the sky in Frontend Integration

It is from constant exposure to customers and comparison with competition that we recognized the trend for ever smaller feature sizes and thus the evolution of the 3rd dimension in our customers' devices.

Apart from the very specific technology developments demanded by individual market segments, we also recognized the needs for "pure play" technology which they all might leverage if we could provide answers to capabilities including trench fillings, via coverages and liners.

An entire program for 300mm Frontend Integration (see article page 42) was therefore created to ensure Evatec remained "on the front foot" for supporting 3D-structures. This was not an application or device. It was an enabling technology that appeared across multiple markets. This program therefore has at its core the goal of providing "building blocks" and a portfolio of solutions that can be tailored to the need of individual customers.

The term 3D Heterogeneous Integration not only includes but also describes both axes contributing to what the community rightly calls the "Essentials", (Figure 3).

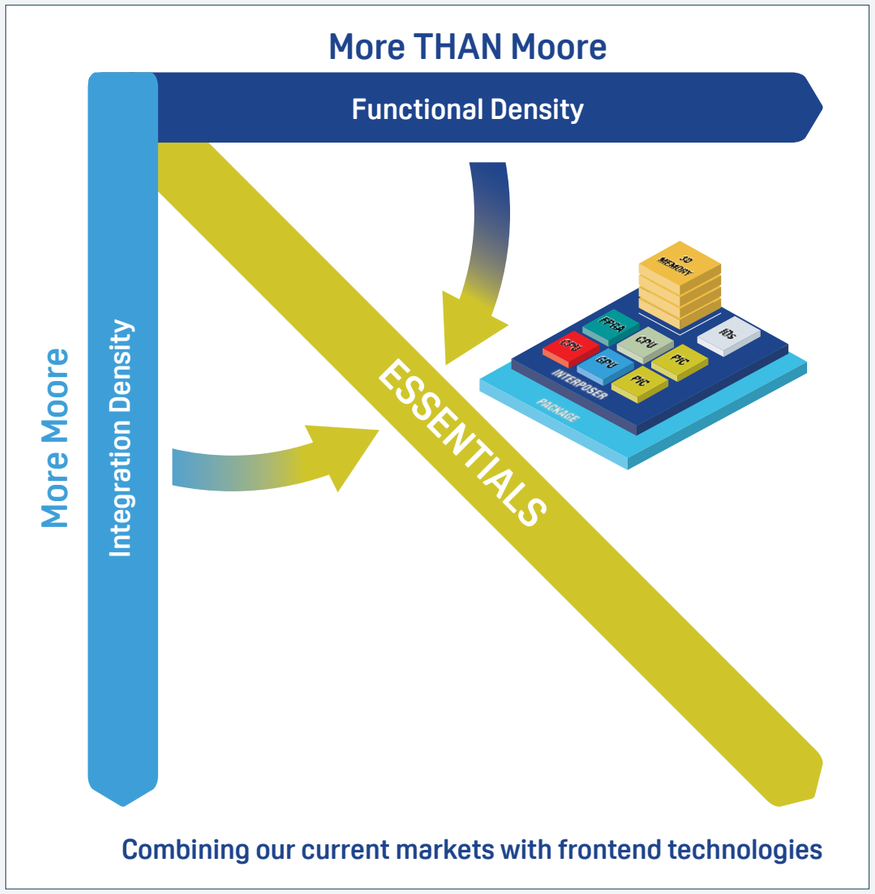

Figure 3: The Big Picture – Innovations for future chips.

It's a balance

These two examples illustrate a subset of conclusions we drew out of the initial Strategy Process. Where the EPIC story comes out of an internal perspective, 300mm Frontend Integration originates in the continuous observation of the market and technology developments. We implemented these findings into our roadmaps and long-term planning whilst still remaining flexible and agile to any emerging customer needs in the shorter term.

From handover to high performance

“Ramp-Up Support” gets you going quicker

David Dietsch, Product Marketing Manager Customer Service, explains how “Ramp-Up Support” helps customers move smoothly from installation to stable production. With hands-on guidance and real-time expertise, this service ensures customer personnel feel confident and ready to unlock the full potential of their new equipment.

Getting started with your new equipment

Bringing a new tool into production is a critical milestone. It marks the point where planning gives way to execution. The tool has been installed, testing completed and “Final Acceptance” signed (FAT). Now, the focus turns to your team who must qualify and release processes and get the tool ready for production.

This phase can be demanding, “go live” with production must stay on schedule, qualification windows are tight, and your internal teams expect clear progress. Engineers begin working with a system they may not yet fully know. Operators need time to build confidence. Process tweaks are still ongoing. Meanwhile, your management is tracking ramp-up milestones closely.

Why “Ramp-Up Support” matters

At this point, customers often realize that questions are still coming up. If small misalignments occur now, they tend to ripple. One overlooked setting or unclear handover process can delay qualification or affect performance. The longer it takes to stabilize the tool, the more it ties up resources and delays the moment when the tool is ready to enter production.

“Ramp-Up Support” brings the clear structures required to this critical phase. Instead of reacting to issues, an experienced engineer is already on-site to guide your team, share best practices, and help your team deliver stable tool performance faster.

Support when it counts

Operators and maintenance staff may already have completed Level 1 and Level 2 training. They know-how to navigate the interface, operate the tool, and follow standard procedures. Still, once the tool enters active production, the environment changes. In many fabs, operators switch between platforms from different suppliers. Handling multiple workflows at once is challenging, especially during the early days of production.

Meanwhile, process engineers focus on aligning tool performance with production goals. What worked during FAT or pre-production testing may need adjusting. Parameters are often fine-tuned to match recipes, workflows, and surrounding equipment.

Even small environmental differences can affect setup. Support is often called for only after progress slows or qualification is affected. With an Evatec engineer on-site right from the start, your team receives timely guidance, clear decisions, and steady support that keeps your project on track.

What's included

Ramp-Up Support gives you direct access to a skilled Field Service Engineer during the early phase of integration. They work closely with your team as the tool moves from installation into qualification and production.

Instead of waiting for issues to be reported and handled remotely, questions are answered in real time by an engineer who is on-site with firsthand knowledge of the issues you want to address.

Adjustments can happen on the spot if parameters need refinement. You gain clarity on how to best run the tool under your specific conditions. In short, Ramp-Up Support helps your team move faster and with more confidence.

"Start-up is always demanding, but with Ramp-Up Support it does not have to be uncertain"

A win for both sides

Customer feedback is clear: Ramp-Up Support makes qualification smoother, and teams feel better supported during a demanding phase. Uncertainty decreases and collaboration improves. The path to production becomes more predictable.

- Fewer unexpected service calls during warranty
- Better planning and fewer delays under pressure
- Faster progress with support already in place
- Direct contact and fast answers build trust

Ramp-Up Support is more than a bridge to production. It's a chance to see what responsive service looks like in daily operations.

Starting strong, staying strong

The first few weeks with a new tool often determine how things will progress.

Teams begin to form routines. Processes take their final shape. Expectations for performance are set. With Evatec Ramp-Up Support, the tool reaches stable performance sooner and your team gains confidence through direct, hands-on collaboration.

So why not reach out to your local Evatec contact to explore how it could support your next project.

The benefits are clear

"Ramp-Up Support" – the benefits

- On-site Field Service Engineer during start-up
- Real-time answers and immediate adjustments
- Support for qualification, setup, and fine-tuning
- Hands-on coaching to reinforce earlier training
- Reduced internal workload and fewer delays
- Standard duration: 3 months, extendable monthly
- Service can be bundled with new equipment or tool relocations

Stefan Marxer

A new chapter in operations

Since joining Evatec at the beginning of 2025, **Stefan Marxer** may still be “the new kid on the block” as COO, but he certainly knows a lot about our industry from the days of his apprenticeship and early career. In his interview, Stefan talks about the current challenges in Operations, how Evatec is tackling them, and what transparency and operational excellence mean in this context.

Stefan Marxer joined Evatec as Chief Operating Officer (COO) in February 2025. Bringing more than 20 years of international experience in operations, including key leadership roles in Asia and Eastern Europe, he offers extensive industry expertise with a strong emphasis on LEAN management and operational excellence. Known for his collaborative leadership style, Stefan is dedicated to driving process standardization and strengthening cross-functional teamwork.

EFFECTIVE TOGETHER

01 Can you remind us how you knew Evatec and what made you interested to join?

I began my career with an apprenticeship as a physics laboratory technician at Balzers AG in 1990 and spent a total of 16 years there, experiencing the company’s transformation through Balzers, Balzers Process Systems, Unaxis, and OC Oerlikon. Since then, I’ve held various operational roles in international companies, including a five-year assignment in Shanghai. Most recently, I had the exciting opportunity to establish a new manufacturing site in Eastern Europe. When I learned about the position at Evatec, I immediately felt that my experience could add real value in strengthening the company’s operational performance.

02 What were your first impressions and how has the business changed since you left the industry back 2006?

The portfolio has grown significantly – not just in size, but also in complexity and technological sophistication. But in many ways “onboarding” felt surprisingly easy. I’ve reconnected with familiar faces and returned to an industry I know well, which made it feel a bit like coming home and helped me get up to speed quickly.

03 What do you see as the challenges for operations from a customer perspective?

It’s clear – speed, quality and cost efficiency. In rapidly changing market situations, our customers need to react quickly to help them take advantage of opportunities so speed at Evatec is essential. At the same time, quality must remain consistently high. It is a key differentiator ensuring high equipment uptime which together with cost efficiency ensures a strong value proposition through cost of ownership. However, these expectations are further complicated by geopolitical uncertainties and export restrictions, necessitating flexible, scalable solutions and adaptable supply chains.

04 How do such challenges affect you internally and what are you doing to address them?

We are currently running several initiatives focused on reducing lead times, lowering manufacturing costs, and maintaining high product quality. These include simplifying internal processes and developing closer collaboration with key suppliers. We’ve also introduced new shopfloor management reporting to increase transparency, monitor key performance indicators (KPIs), and ensure we take immediate corrective actions when needed. A dedicated task force helps us respond quickly to supply chain disruptions and set clear priorities to ensure continuity.

05 Many people talk about “Operational Excellence”. What does that term mean to you?

For me, Operational Excellence means delivering consistent, efficient and reliable performance in daily operations. It focuses on optimizing procurement, inventory management, logistics, and supplier performance to reduce lead times and costs, while fostering a culture of continuous improvement. Ultimately, it’s about ensuring material availability, minimizing operational costs and delivering high-quality results in a sustainable way.

06 What role does transparency and data play in improving and tracking Evatec’s operations processes?

Transparency is key to success. Without clear data, you can’t take the right actions or measure progress. That’s why we’ve introduced visible shopfloor boards that display KPIs and relevant information. We’re also driving digitalization initiatives to track tools in assembly across the value chain and gain better insights into productivity.

07 How do you see the role of AI to support you in the future?

AI is becoming increasingly important across many areas. We’re currently rolling out a software solution that uses AI to support business processes like order confirmations, delivery notes, and invoices. It also helps improve the quality of master data in our ERP system. As part of this initiative, we’re implementing key processes such as Purchase-to-Pay (P2P) and Order-to-Cash (O2C).

08 How do you keep your team motivated and working effectively together?

It’s all about being a team and pulling in the same direction. In March this year, we held a two-day workshop to define our strategy, KPIs, and the actions needed to reach our goals. This collaborative approach created strong alignment and ownership within the team. At the heart of our daily activities is the principle of working ‘Effective Together’, a slogan we launched to reflect our commitment to collaboration, and leadership. Regular communication, clear responsibilities, and recognition of achievements help maintain motivation and team spirit high. A big thank you to my team for the welcome and what we achieved together already!

“The challenges are clear – speed, quality and cost efficiency”

Going big in Japan

As Evatec's business in Japan continues to develop so does our organization. Evatec Japan Managing Director, **Seiji Hirai**, tells us about the recent organizational changes and how they help us deliver the local support our customers expect.

Evatec Japan at a Glance

Company Name: Evatec Japan Ltd.

Key Contact:
Seiji Hirai, Managing Director

Tel: +81 6 4708 8750

Head Count: 12

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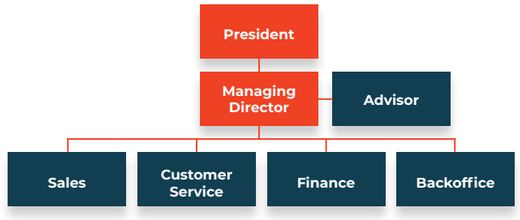

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After studying materials science, **Seiji Hirai** started his career in 1998 working as a Field Application Engineer in Balzers, Unaxis, and Oerlikon. Before joining Evatec, he served as a Sales and Business Development Manager for Swedish and German manufacturers of assembly and metal processing machinery in the automotive, aerospace, and electronics sectors. He focused on expanding their business in Japan.

01 Can you tell us a bit about your role as Managing Director of Evatec Japan?

My job is to use my most recent work experience managing capital equipment sales into Japan and combine it with previous know-how from the thin film industry to help Evatec now build its business further in Japan.

Since stepping into the role of Managing Director in February this year, I've taken time to understand our current position and identify opportunities for growth. Previous thin film experience in the rewritable optical disc market showed me that we could achieve a dominant position for our Swiss brand in Japan with a market share of around 90% by offering exceptional customer service and high-quality equipment. With a clear vision, stand out high quality products from Switzerland and the best local support organization for customers, I am confident we can also now grow the business of Evatec Japan too.

02 Tell us about your local organization and its strengths.

We take care of everything from equipment sales, to all the daily service support our customers expect – from initial installations, to daily on-site or remote production support and upgrades.

Our order processing and finance team is there to make sure everything runs smoothly. I see it as a very flexible, agile local organization enabling us to place the right people in the right roles at the right time. Colleagues from headquarters and other global teams have not only joined daily Teams meetings but also visited customers on-site since our local Evatec Japan organization was first founded. This has helped build strong trust, the skills and motivation of our team. Looking ahead to ongoing major equipment start-ups in Japan we will use this good collaboration and teamwork to ensure successful project completions before year end. I believe Evatec's strength lies in its ability to deliver expert customer support, not only through Evatec Japan, but as a wider team in close collaboration with our Swiss headquarters and other Asian teams.

03 What is Evatec Japan's main market focus?

It's an exciting time. Evatec has been working successfully through local partner Canon Marketing since 2016 developing its business for semiconductor PVD solutions. Evatec Japan was then set up in 2019 and has been focused more on starting the work building the Evatec brand in the Photonics and Advanced Packaging markets. However, as the worlds of semiconductors and photonics increasingly overlap we need to leverage synergies and know-how across different markets. It's time to put all the business activities together under one roof at Evatec Japan, effective February 2026.

For Japanese customers that brings important advantages:

- One single local Evatec organization serving all markets in Japan
- Direct communication with one team on their interests across several markets
- Easy access to the global service team

04 What makes the Japanese market interesting for Evatec?

We are a good fit as Evatec can offer solutions in specialized markets where Japan has a longstanding reputation for technology leadership. The importance of quality design, manufacturing, and long product life is a shared interest in both our societies.

Evatec's approach adapting carefully to specific customer needs means we can deliver solutions where other players struggle to offer the same level of flexibility and customization.

By working closely with our customers sharing technical planning and samplings, and by tightly integrating our local efforts with the technical expertise of our headquarters, we position ourselves as a trusted consultant and solution provider in these specialized segments.

05 What are the challenges Evatec faces in the Japanese market, and how is it different from other markets?

In Japan, customers demand rigorous confirmation and validation of equipment specifications to ensure the production of highly reliable semiconductor products. Simply presenting strong catalog specs is not enough to secure business. Detailed discussions – known as Suriawase (alignment and adjustment) – are essential to ensure that the equipment and processes developed at our headquarters meet the exact requirements of Japanese customers. Even the reasoning behind technical decisions is closely examined.

Evatec Japan plays a key role in bridging cultural and technical gaps, facilitating smooth communication and project alignment between customers and our Swiss headquarters.

06 How do you collaborate with other Evatec locations around the world?

The ongoing shortage of Service and Application Engineers is a major challenge in the semiconductor equipment industry, especially in Japan, where recruiting skilled talent is particularly difficult.

On top of that, project workloads fluctuate significantly between peak and off-peak periods. To manage this, we rely on a global support network of engineers who are trained to work seamlessly together and share a common culture. This collaboration helps us stay flexible and maintain high service quality during busy times.

07 How do you see the Japanese Market developing and what opportunities will that bring for Evatec?

We see strong growth in Advanced Packaging as a major step forward for Japan's semiconductor industry and a key opportunity for Evatec. Once overshadowed by wafer processing, the role played by packaging in enabling new technologies and devices to be manufactured cost effectively is growing. New chiplet architectures, new materials, and innovative methods are creating fresh demand for advanced deposition solutions. Evatec aims to support this shift by offering wafer and panel level technologies tailored for OSATs in Japan.

In parallel, the rise of AI semiconductors is driving demand for improved Power Devices, whilst the potential growth of application areas like Augmented Reality will drive the need for enhanced Optoelectronics. With our expertise in controlling both electrical and optical performance of thin films, our capabilities to manage heat dissipation & stress control within substrates, and our thin film know-how supporting build of 3D structures we believe Evatec is well positioned to support all these emerging needs.

"It's an exciting time – our business in Japan is growing strongly"

08 What are you most excited about for the future of Evatec Japan?

What excites me most is the strength and long experience of Evatec's global management and development teams. Many talented colleagues I worked with at Oerlikon Systems before 2008 have since been reunited at Evatec, and meeting them all again when I started was truly inspiring. I believe that a capable and well-aligned team, not just with knowledge and technology, but with a shared vision, can create real value.

Our goal is to build a "Dream Team" in Japan that not only promotes our advanced technologies and equipment, but also strengthens the Evatec brand and expands our presence in the Japanese market.

Keeping cool with the hottest technology

PVD epitaxial growth on CLUSTERLINE® 300

While MBE offers excellent results in crystalline film quality, its low deposition rates limit its suitability for high-volume applications, but now it looks like we have a solution. Evatec Project Manager, **Markus Mueller**, tells us the story of what's been achieved so far and what's to come.

Figure 1: First demonstrator equipped with 4 FTC sources in the Evatec Competence Laboratory

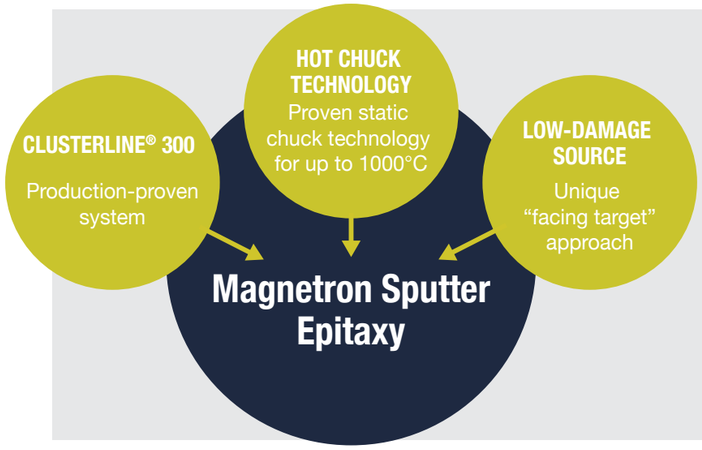
Understanding the challenge

New Evatec developments in "hot chuck" and "cathode" technology look set to enable epitaxial and quasi-epitaxial growth using PVD-based processes, delivering practical production solutions for a wide range of advanced functional materials, including BTO (Barium Titanate), GaN (Gallium Nitride), ITO (Indium Tin Oxide), and LNO (Lithium Niobate).

The first thing we had to do was sit down with customers and set clear goals. Depositing crystalline films with high uniformity was a prerequisite, but we also needed to understand more about the typical materials and film thicknesses they would need in future, the acceptable levels of contamination, the throughput requirements, and other possible limitations we needed to overcome to make a PVD based solution an attractive one for the future. Figure 2 illustrates some typical process requirements. Beyond film uniformity, the system had to be designed to fulfill additional frontend fab specifications.

- **Substrate Temperature:** Up to 750°C
- **Rocking Curve:** < 0.6° (FWHM)
- **Film thickness uniformity:** < 3% (1 sigma)
- **Deposition rates:** > 40nm/h

Figure 2: Four process challenges



CLUSTERLINE® 300 as the basis

The production-proven fab compatible CLUSTERLINE® 300 platform was our starting point. Our approach was to develop a modular PVD solution achieving crystalline growth by combining elevated substrate temperatures with low-damage deposition techniques. A key philosophy was to build on existing know-how wherever possible, further developing and optimizing existing production-proven component parts to shorten development times and minimize risk.

Figure 3: Inside the heart of the chamber - Rotary 12" Chuck with dual zone SiC below.

Very Hot Chuck Technology

The central element was the very hot rotating chuck where Evatec built up lots of know-how over the last few years, especially when it comes to contamination reduced designs based on SiC heater elements. The newly designed chuck (Figure 3) heats 12" wafers up to 750°C with a temperature uniformity of ±2% to support crystalline growth processes. Working in combination with the modified Facing Target Cathode (FTC) source (see Figure 4), it also rotates during deposition to ensure the dynamic averaging required to meet strict film performance targets for layer properties across the substrate. Meeting these combined requirements takes precise coordination of thermal control, mechanical design, plasma optimization, and particle control, all integral parts of the overall system concept.

Handling high process temperatures in a vacuum chamber presents several challenges. Many peripheral components, such as feedthroughs, sensors, or the sources are limited to maximum temperatures. To stay within these boundaries, the development team combined:

- Thermal shielding and clever layout
- Active and passive cooling concepts
- The use of temperature-resistant materials

Since radiation is the dominant heat transfer mechanism in ultra-high vacuum, material selection for emissivity and thermal stability is a key part of the design. A dual-zone heater is used to ensure uniform temperature control across the wafer, while the cooling strategy is carefully balanced to prevent localized cold spots near the substrate.

Facing Target Cathode (FTC) Technology

The deposition source is based on Evatec's established Facing Target Cathode (FTC) technology. The new updated design integrates four independently controlled FTC sources (eight targets total), arranged and tuned using extensive plasma simulations. This setup allows optimization of both thickness uniformity and deposition rate. Additionally, new RF and DC generators, combined with customized matching units and gas control, are being used to fine-tune process conditions.

Working at high temperatures up to 1,200°C at certain surfaces requires all components to be selected for minimal outgassing and diffusion. This necessitates the use of rare or difficult-to-machine materials with high thermal stability, while still meeting the temperature uniformity requirements. To further reduce particle generation, sources and shielding have also been refined to minimize particle load and improve serviceability while the design needs to allow for simple target exchange in production.

Bringing it all together

Extensive performance simulations and actual component testing on 200 and then 300mm have been at the heart of the development work (Figures 5, 6 & 7).

Solutions on 300mm are coming soon. The 300mm hardware will be ready for customer samplings within our Evatec Competence Laboratory (ECL) in Q2 2026.

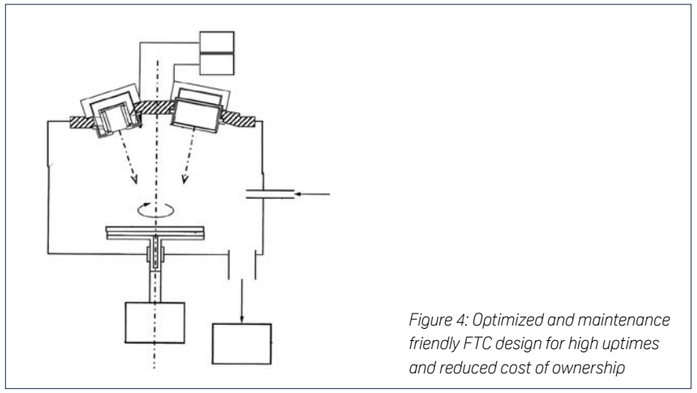


Figure 4: Optimized and maintenance friendly FTC design for high uptimes and reduced cost of ownership

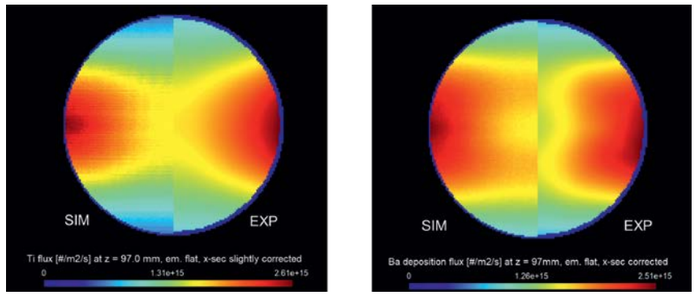


Figure 5: Feasibility studies and samplings validated simulation results.

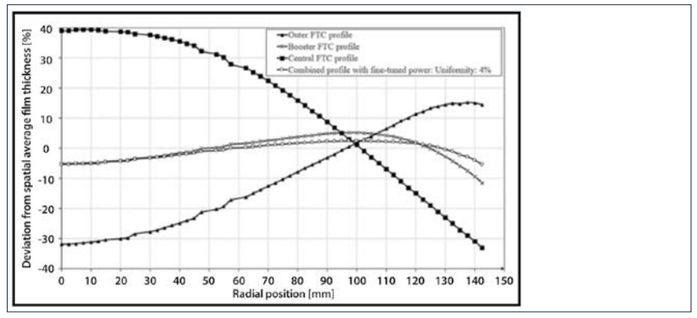


Figure 6: The arrangement of the FTCs combined is only one of the tuning nobs - but a major one.

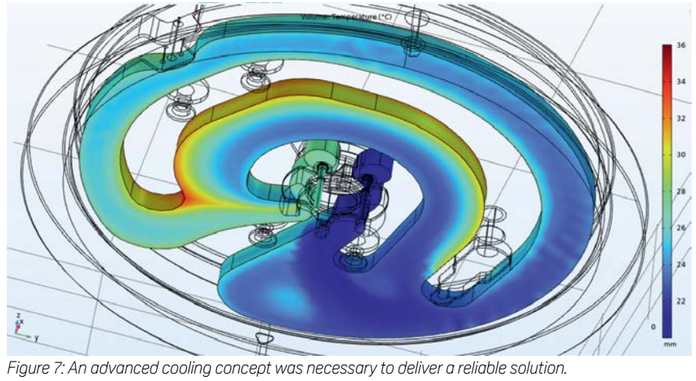


Figure 7: An advanced cooling concept was necessary to deliver a reliable solution.

PEALD

The smartest plasma, the purest films

Dr. Julian Pilz and **Shiv Jyotindra-Bhudia** of Silicon Austria Labs and **Dominik Hartmann**, Manager Technology Development at Evatec, report recent results showing how a novel Microwave Electron Cyclotron Resonance (ECR) Plasma Source delivers Ultra-Pure, Damage-Free films in Plasma Enhanced Atomic Layer Deposition (PEALD).

Why PEALD

PEALD has become a key technology in the semiconductor industry to produce advanced electronic and structural thin films in the nm range. However, when film purity, low-temperature growth and structural control are all required at once, conventional plasma sources often reach their limits. In LAYERS 8, Evatec introduced its new PEALD module for integration on CLUSTERLINE® 200 and highlighted the benefits of ECR source technology. Now we can report recent results demonstrating the system's ability to meet key industry demands by enabling the production of ultra-pure Al_2O_3 for advanced gate dielectrics in logic and memory devices, as well as highly crystalline AlN films for piezoelectric MEMS, thermal interface layers, and dielectric components for RF and power applications.

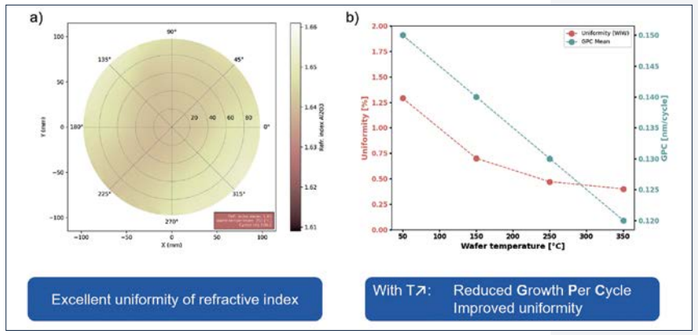


Figure 1: Single wafer process Al_2O_3 layer characteristics. a) The refractive index map is shown for the 250 °C process, which shows excellent uniformity across the entire wafer at a refractive index of 1.65 in most areas. b) The thickness uniformity and GPC as a function of temperature illustrate how uniformity gets better, while GPC decreases at increasing temperature.

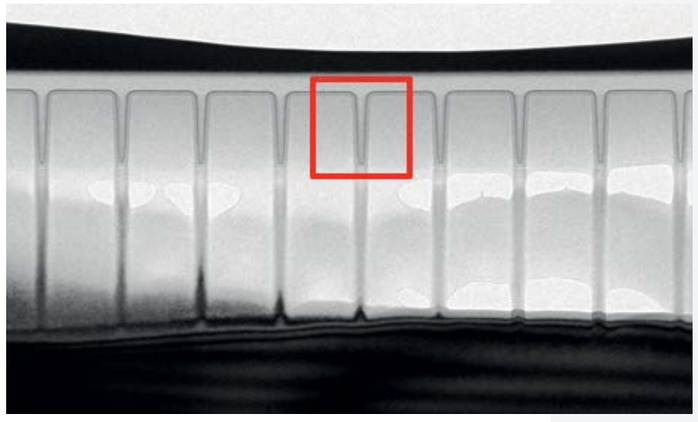


Figure 2: a) TEM measurements of Al_2O_3 on high aspect ratio structure, Large scale image of multiple vias.

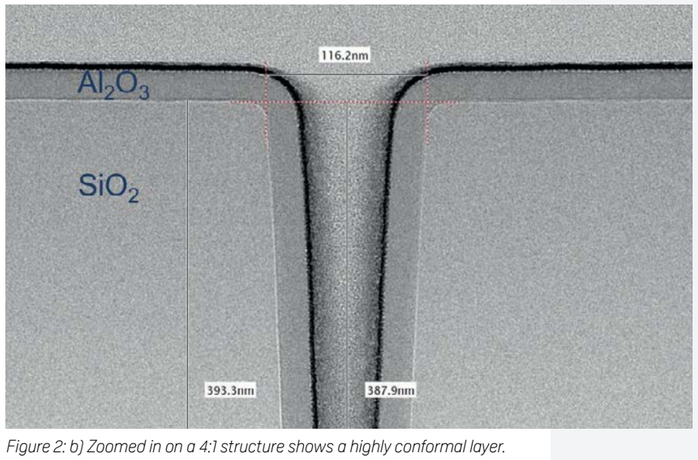


Figure 2: b) Zoomed in on a 4:1 structure shows a highly conformal layer.

Al_2O_3 - Precise layers and high throughput

Single wafer processes, where Al_2O_3 is deposited for 25 wafers in a batch, shows excellent thickness uniformity across the 200 mm silicon substrates, with variations below 0.5% and stable refractive index values around 1.65 at 633 nm.

At a growth rate of 1.8 nm/min, 50 nm Al_2O_3 coatings can be processed in under 30 min, leading to the entire batch processed within half a day, while in-film particle (>0.3 µm) generation is kept low at < 50. Figure 1 illustrates how the refractive index, thickness uniformity and growth per cycle (GPC) behave as a function of temperature showing that elevated temperature can smoothen and densify the Al_2O_3. This can be helpful in applications such as hydrogen diffusion barriers.

Micrographs in Figure 2 also show how the process can deliver highly conformal coatings, with high aspect ratios > 4:1. Pre-etched SiO_2 structures were coated with 20 nm of Al_2O_3, showing that the same throughput could also be achieved on structured wafers with outstanding conformality.

AlN Films – High purity and tuneable crystallinity

Aluminium nitride is a key material in advanced microelectronic devices. It is used in piezoelectric MEMS, thermal interface layers and dielectric components for RF and power applications [1, 2]. Material quality is of the highest importance, and especially crystallinity, stoichiometry, and impurity levels which have decisive impacts on the device performance [3].

Highly oriented AlN films are typically grown using methods such as metalorganic chemical vapor deposition [4] or reactive sputtering [5]. However, these approaches often lack the process control and integration flexibility needed for modern device architectures. Whilst Plasma-enhanced atomic layer deposition offers a promising alternative [6-8], the challenge there has been to achieve similar structural quality while keeping oxygen and carbon impurities to a minimum [9, 10].

In these trials, we used our newly developed microwave-based PEALD system to grow AlN on 200 mm Si (111) wafers. The process combines trimethylaluminum (TMA) with ammonia (NH_3) plasma. The high-density microwave plasma allows precise tuning of energy input by varying the microwave power between 50-500W. Furthermore, various other parameters in the process, such as pressure, NH3 flow, and exposure time can be individually adjusted to tune the desired properties. This gives full control over film growth, chemistry and structure.

Figure 4 shows the layer characteristics as measured by ellipsometry at 633 nm. In Figure 4a, thickness uniformities <1% can be achieved at T = 200°C (chuck temperature) for a 500 cycle process. The refractive index uniformity is illustrated in Figure 4b. The wafer shows polycrystalline regions especially in the outward regions, which can be identified from high refractive indices > 1.9.

X-ray photoelectron spectroscopy (Figure 5) confirms excellent purity, where oxygen and carbon levels are extremely low and almost not detectable. Figure 5 shows the bulk composition of AlN grown with different plasma cycle doses at different radial positions on the wafer. To compare the composition, the reference values for bulk AlN are also shown on the right side. Of significant note is that the AlN structure has reached an almost identical composition to the bulk reference case after only 10 s, which proves its exceptional quality. There is

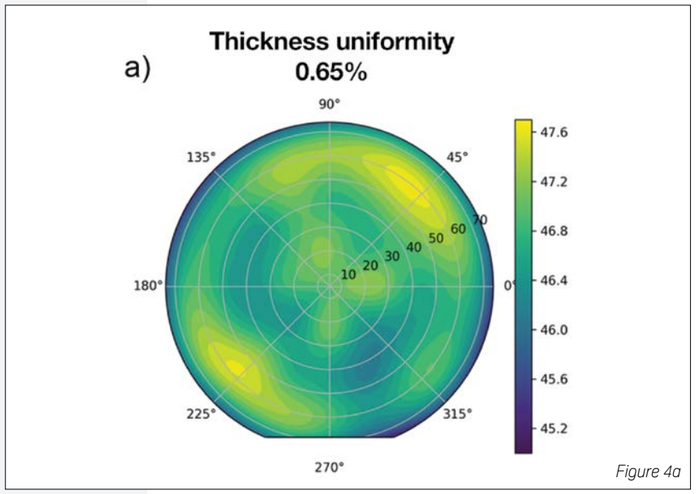


Figure 4a

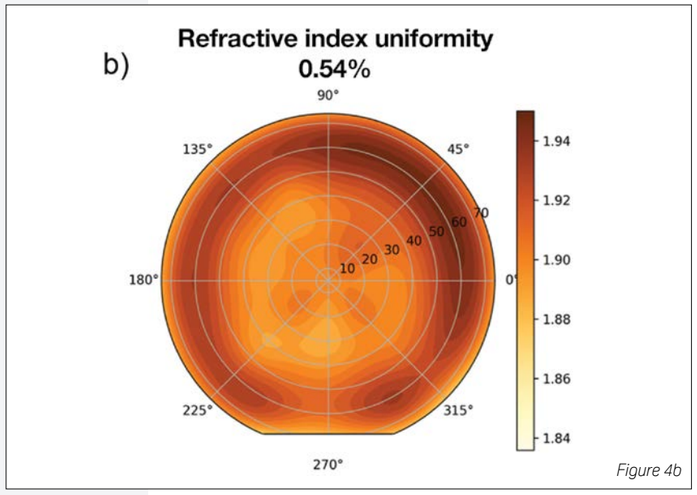


Figure 4b

Figure 4: AlN layer characteristics measured by ellipsometry at 633 nm. a) Thickness uniformity
b) Refractive index uniformity. Process: 200°C, 500 cycles.

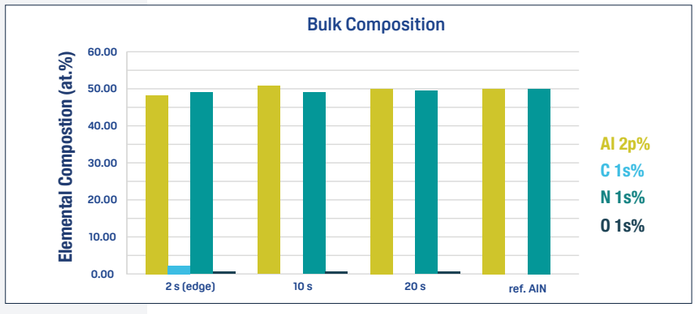


Figure 5: Elemental composition of AlN measured by XPS for different plasma times on different radial positions of the wafer. After 10s there is no C detected anymore, which is an excellent proof of high quality PEALD environment. There is only a minimal amount of oxygen detected, which is due to surface oxidation. As a reference the AlN elemental ratios (1:1) are shown.

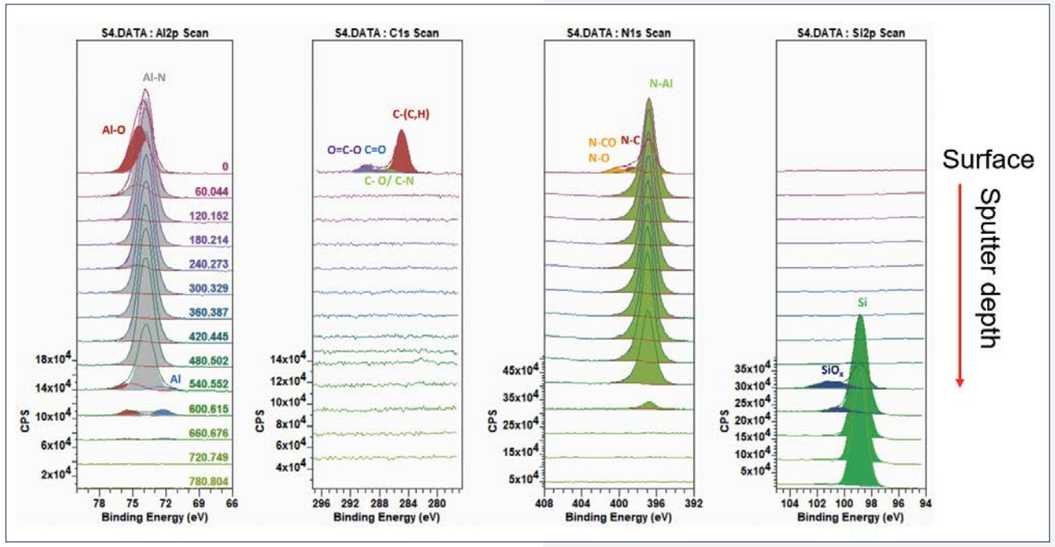


Figure 6: XPS depth profiles shown for Al, O , N, and Si. The number in different colors form purple to green show the sputter times. There is no detectable C in the bulk of the material (second plot), which is a great sign of quality nitride layers.

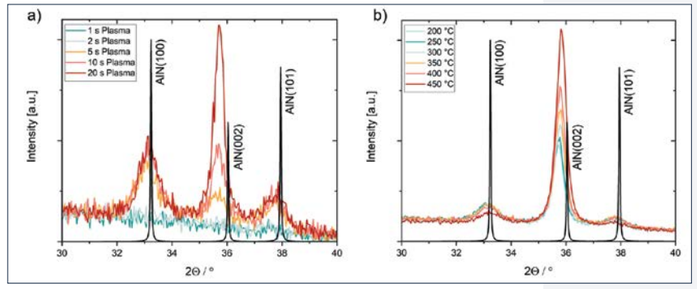


Figure 7: XRD Grazing incidence scans of processed AlN layers with different plasma times (a) and at different temperatures (b).

References: [1] La Spina, L. et al., Solid-State Electronics, 1359–1363 (2008). [2] Haider, S. T. et al., IEEE Access, 58779–58795 (2023). [3] Strnad, N. A. et al., Journal of Vacuum Science & Technology A, 40(4) (2022). [4] Demir, I. et al., Journal of Physics D: Applied Physics, 51(8), 085104 (2018). [5] Dadgar, A. et al., Physica Status Solidi (a), 220(8), 2200609 (2023). [6] Österlund, E. et al., Journal of Vacuum Science & Technology A, 39(3) (2021). [7] Ueda, S. T. et al., Journal of Materials Chemistry C, 10(14), 5707–5715 (2022). [8] Goswami, R. et al., Coatings, 11(4), 482 (2021). [9] Zhang, X. Y. et al., Journal of Materials Research and Technology, 27, 4213–4223 (2023). [10] Gungor, N. & Alevli, M., Journal of Vacuum Science & Technology A, 40(2) (2022). [11] Lau, W. S. et al., Applied Physics Letters, 87, 123505 (2005). [12] Manzeli, S. et al., Nature Reviews Materials, 2, 17033 (2017). [13] Radisavljevic, B. et al., Nature Nanotechnology, 6, 147 (2011). [14] Chowdhury, S. & Mishra, U., IEEE Transactions on Electron Devices, 60, 3060 (2013).

only minor surface oxidation caused by post-deposition air exposure. Depth profiling (Figure 6) further confirms that contamination is confined to the surface, highlighting the cleanliness and reliability of the process. We have further analysed the crystal structure using X-ray diffraction. Figure 7a shows that increasing the ammonia plasma duration enhances the (002) peak intensity, indicating stronger c-axis texture. This trend continues with higher substrate temperatures, as seen in Figure 7b. Even at just 200 °C the tool delivers highly oriented films. This level of control enables fabs to adapt the process to match their device and integration needs.

Process integration on a single platform

One of the main advantages of the Evatec PEALD system is its integration into the CLUSTERLINE® 200 platform, where it can be combined with PECVD, sputtering, and plasma etching technologies without interrupting the vacuum process throughout the entire process flow. This configuration enables complete, multi-step device fabrication without exposing the wafer to ambient conditions.

Surface pretreatment, seed layer deposition, film growth and encapsulation can be carried out in a connected and controlled vacuum and process flow. This high degree of integration opens new options for advanced device fabrication, e.g. high-κ metal gate stacks (HKMG) benefit from clean, sequential deposition of dielectrics and metals in one tool environment [11]. 2D materials like MoS_2 and graphene need damage-free surface pretreatment and careful encapsulation to retain their electrical performance [12,13]. GaN on diamond for high power devices relies on low-temperature, conformal coatings with tight interface control [14]. VCSELs and Micro-LEDs require precise control of multilayer thickness and stress for optimal optical performance.

Figure 8 shows a possible configuration of the CLUSTERLINE® 200 with PEALD, PECVD, sputter, and etch modules connected to a central wafer handling system. Each module can be adapted for specific materials or coating processes. Depending on requirements, the system can be equipped with multiple PEALD modules with numerous precursor lines.

So what's next?

The Evatec team is already exploring advanced materials such as AlScN, InGaN etc. and how a newly developed RF chuck can tune crystallinity and other important properties through super-cycle processing. With all these capabilities in one platform, we are ready to support our customer's innovations in logic, power devices, optical coatings, optoelectronics and sensor technologies from R&D to high-volume manufacturing.

Acknowledgement:
XPS measurements have been performed at the Luxembourg Institute of Science and Technology.

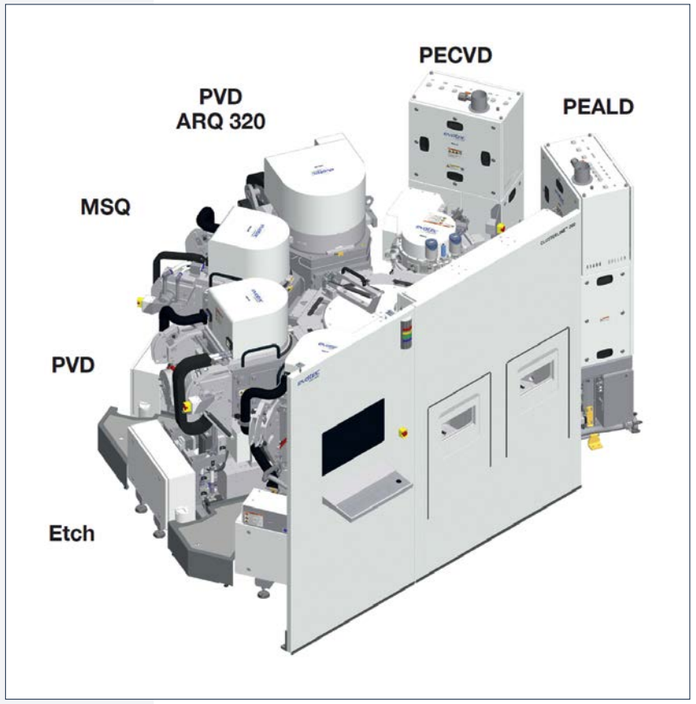


Figure 8: CLUSTERLINE® 200 combines many advanced technologies for advanced device fabrication without breaking vacuum.

"With this new platform, Evatec brings a highly flexible and scalable PEALD solution to the market. It delivers high-purity, crystalline AlN films on full 200 mm wafers. The tool is ready to support a wide range of applications, from next-generation piezoelectric components to thermal and dielectric layers in RF and power devices. For customers looking to combine high performance with process control, this system offers a clear path forward"

Dr. Julian Pilz, Silicon Austria Labs (SAL)

Innovations and Opportunities

in Panel Level Packaging

Things are moving fast in the world of Panel Level Packaging. **Mohamed Elghazzali**, Manager Technology Development, **Stanley Low**, Product Marketing Manager, and **Admir Asanoski**, Head of Semiconductor & Advanced Packaging, expand on Evatec strategy and roadmaps, making sure our market offerings can address the full spectrum of customer requirements.

Advanced Panel Level packaging enables higher bandwidth and improved thermal management, both of which are critical for AI chiplets. Moving from Wafer Level Packaging (300 mm wafers) to panel formats such as 310x310 mm, and extending solutions to larger areas up to 650x650 mm, is part of the evolution that Evatec is ready to enable with its platforms.

Evatec's CLUSTERLINE® platform is already established for high-volume deposition and etching in wafer and panel manufacturing. Building on this foundation, we are extending the platform's capabilities to meet the new requirements of advanced packaging. Our roadmap covers three key areas where we are investing and developing future solutions.

Building on a proven base

The Panel Level Packaging (PLP) market is entering a phase of rapid growth and innovation, driven by modular chiplet architectures for AI and high-performance computing. Evatec has been shaping the future of Panel Level Packaging from the very beginning. Almost a decade ago, when this new market segment first emerged, Evatec pioneered panel level PVD solutions right from the start. Today, the company is leveraging its long-standing expertise and strong market presence to drive the next wave of innovation. With a comprehensive roadmap in place, Evatec is continuing to adapt its technologies and product portfolio to the latest developments and future trends, starting from the first projects on 310x310 mm panel formats, then advancing towards even larger panel sizes.

Our activities focus on redistribution layer (RDL) and backside metallization (BSM), through-glass via (TGV) technologies, and reactive ion etching (RIE) for PCB and IC substrate manufacturing.

RDL and BSM roadmap for AI chiplets

Evatec has launched its first dedicated PLP development project for the 310x310 mm format starting from the CLUSTERLINE® 300 platform. This modified system is being engineered to handle and transport panels efficiently, providing higher substrate utilization per cycle compared to 300 mm wafers. Such scaling will allow larger AI chiplets and high-bandwidth memory (HBM) stacks to be processed, boosting throughput and reducing cost per chip.

The development includes new DC/RF sputter and etch modules, a high-performance source and magnet system, and in-situ process control for maximum uniformity and optimized material use. Capabilities under development also target precious metal deposition such as gold with focus on reducing target costs.

The 310x310 mm solution is expected to be available to foundries and OSATs by 2026. In parallel, Evatec is preparing cost-optimized solutions for larger panel formats on the CLUSTERLINE® 600, supporting sizes up to 650x650 mm.

Evatec solution of optimal efficiency

Wafer	Panel	Platform
300 mm		CLUSTERLINE® 300
	300x300 mm	CLUSTERLINE® 310
	310x310 mm	CLUSTERLINE® 310
	510x515 mm	CLUSTERLINE® 600
	600x600 mm	CLUSTERLINE® 600

TGV technology roadmap for large panels

Glass interposers are becoming essential for high-frequency and RF packaging. They require precise drilling, metallization, and dielectric gap filling. Evatec's CLUSTERLINE® 600 platform is being prepared for advanced thin-film deposition on large-area glass substrates.

The roadmap foresees adhesion layer and copper seed layer deposition for TGVs with aspect ratios up to 6:1, with future enhancements aiming beyond 10:1. Ionized plasma capabilities will support conformal adhesion and copper coverage along the sidewalls enabling robust interconnect performance.

In addition to deposition modules, the roadmap includes process integration, automated metrology, and advanced panel-handling concepts (such as enhanced flipper systems) to deliver a complete TGV processing solution for panels up to 600 mm.

RIE and Desmear roadmap for PCB/IC substrates

For organic, polymeric, and glass substrates, Evatec is extending its technology base with plasma etching and desmear solutions. The CLUSTERLINE® 600 and the CLUSTERLINE® 310 with integrated CCP etch modules and atmospheric batch degassing will support advanced substrate pre-treatment.

Planned configurations will enable deep via etching with high aspect ratios and desmear processes optimized for polymer and SiO_2 fillers. Balanced chemistries and Arctic cooling techniques will ensure residue-free via walls, reliable copper adhesion, and repeatable performance across large panels. These developments will provide customers with scalable, production-ready solutions for the evolving demands of advanced PCB and IC substrate manufacturing.

Outlook

With the 310x310 mm project underway and larger-format developments in preparation, Evatec is establishing a roadmap that addresses the full spectrum of future PLP requirements.

Our CLUSTERLINE® platforms will continue to evolve as flexible, high-volume manufacturing solutions, supporting customers as they move from wafer-based packaging to panel formats of increasing size and complexity.

Welcome to **Advanced Directional Sputtering (ADS)**

Evatec's Senior Program Manager, **Kai Wenz**, introduces the latest PVD technology capability in Evatec's portfolio and gives us a flavor of some of the markets where the enhanced capability can help deliver new levels of device performance.

Conventional PVD – an industry workhorse

Standard physical vapor deposition (PVD) sputtering is a workhorse technique across all Evatec market segments. In the conventional way, atoms are ejected from a target by energetic ion bombardment and travel towards the substrate in a largely random, isotropic distribution. For planar films or shallow topographies, this solution works well - deposition is fast, uniform, and cost-effective. However, as device architectures have evolved toward smaller geometries, higher aspect ratios, and increasingly 3D layouts, the limitations of standard sputtering have become apparent. In deep features such as through vias, or trenches, Isotropic particle flux tends to:

- Deposit excessively on feature sidewalls, narrowing or closing the opening before the bottom sidewalls are coated.
- Increase the probability of voids.
- Result in incomplete or discontinuous bottom coverage, leading to electrical open circuits or high resistance.

Solving the 3D and high aspect ratio challenge

Directional sputtering addresses these challenges by engineering the angular distribution of sputtered atoms so that they arrive predominantly at almost vertical incidence on the substrate surface. This is achieved using methods such as:

- **Collimated sputtering:** Placing a physical collimator between the target and the substrate to filter out off-angle atoms.
- **Ionized PVD (I-PVD):** Ionizing a significant fraction of the sputtered flux and using an electric field to direct it straight into the features.
- **Long-throw sputtering:** Increasing target-to-substrate distance to naturally narrow the angular spread of incoming atoms.

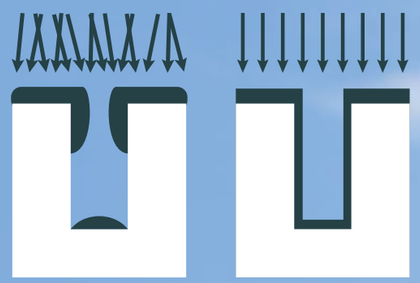


Figure 1: Conventional vs directional sputtering.

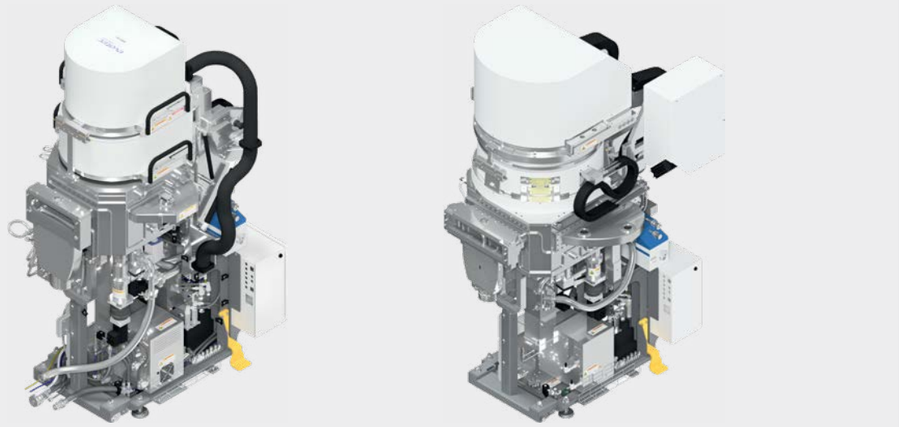
The Evatec solutions – SDS and ADS

Evatec's ADS stands for Advanced Directional Sputtering and is available for the CLUSTERLINE® 200 and 300 platforms.

ADS is a key development focus for our new frontend capabilities, allowing high productivity with shutter, RF Bias, hot and cold electrostatic chucks at very low particle and metallic contamination levels. For less challenging structures, aspect ratios and technology nodes the simplified SDS (Standard Directional Sputtering) setup with fewer tuning features is available for cost effectiveness.

Key materials are Ti/TiN, Ta/TaN, and Cu, but it can be used and optimized for other materials too.

In today's advanced manufacturing landscape, where structures can be smaller, pitches tighter, and sometimes deeper, with higher performance demands, directional sputtering has moved from a specialty process to a critical enabler. Without it, many state-of-the-art metallization steps in high-performance computing, 5G, and AI (artificial intelligence) hardware would not be manufacturable at volume with the required reliability.



ADS 200 solution for 200mm processing

ADS 300 solution 300mm processing

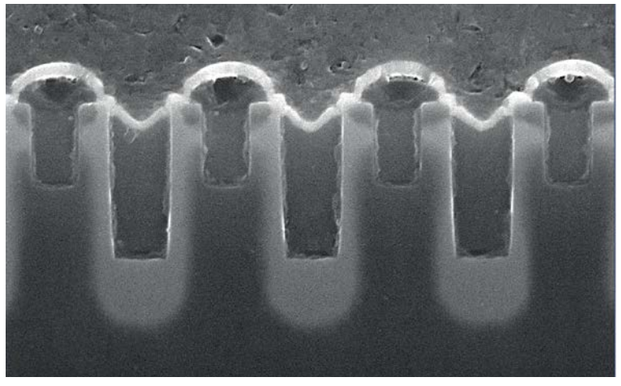
Figure 2

ADS in action

Here are just four application examples where directional sputtering is essential in supporting our customers and their needs:

1. Power Discrete

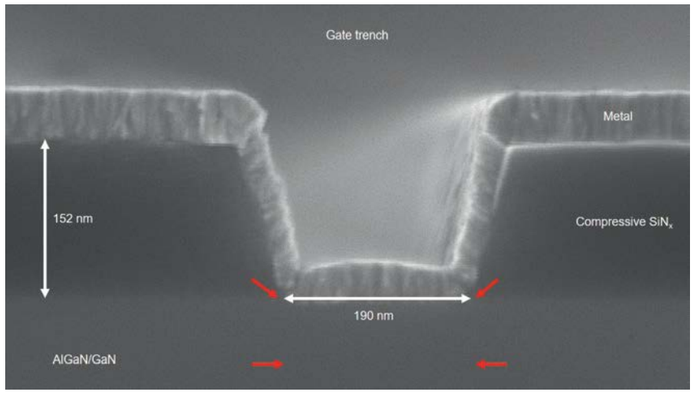
In trench MOSFETs and IGBTs, Ti/TiN layers must form a continuous adhesion and diffusion barrier deep inside high-aspect-ratio trenches. Standard sputtering often causes sidewall overhang and poor bottom coverage, leading to high resistance and reliability issues. Evatec's ADS solution overcomes this challenge.



Sic Mosfet Gate Design - Die Cross Section, SEM View from Rohm Semiconductor – Source: SiC Transistor Comparison 2023 report, Yole Group

2. Wireless

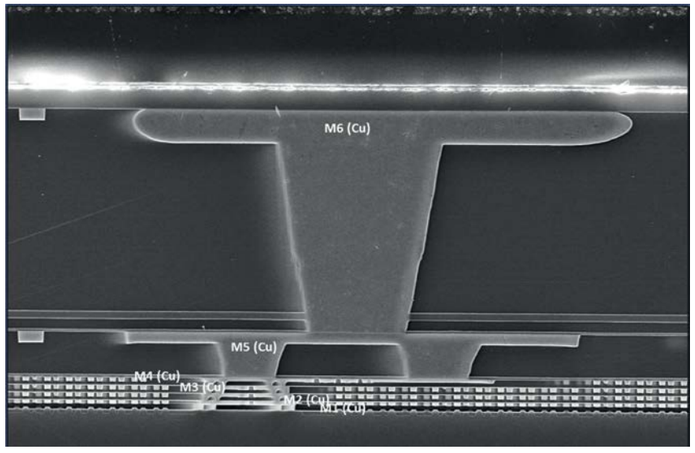
GaAs-based HBTs and HEMTs are the most commonly used technologies for RF power amplifiers. These devices require conformal coatings of metals like WTi, Cu, Au, and Ti, especially Ti/Cu and Ti/Au bi-layers, where Ti serves as a seed layer and Cu or Au as the conductor. ADS technology provides superior conformality and step coverage compared to traditional sputtering, enabling damage-free deposition on complex structures. Its precise plasma control and low ion energy ensure excellent film uniformity and adhesion, enhancing device performance and reliability in demanding RF environments.



BCD 90MN Cross-Section: Thick metal layer in cross-section - SEM view Exploration of high-temperature PECVD SiNx for strain engineering of GaN-HEMTs | Ferdinand-Braun-Institut. Image courtesy of © FBH

3. Frontend

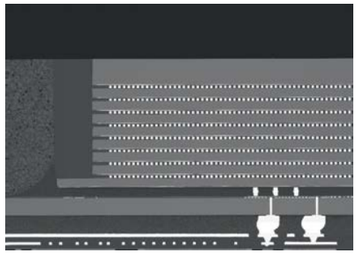
In advanced interconnect fabrication, liner, barrier layers, and seed layers must be continuous and uniformly coated on the sidewall. Depending on the architecture, coating at the bottom may also be required for connection to other features underneath. Typical materials used are Ti/TiN-Al (200 mm) reflow or TaN/Ta-Cu (300 mm) enable void-free Cu electroplating. Typical structures used are contact holes, trenches and dual damascene features. With the trend to smaller structures new materials are under evaluation and the number of interconnects continues to increase.



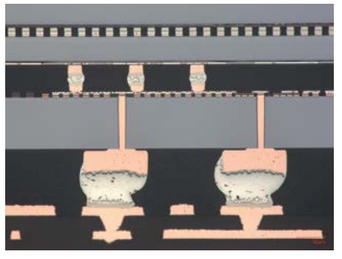
BCD 90nm Cross-Section: Thick Metal Layer In Cross-Section - Sem View
Source: BCD Comparison 2024 Report, Yole Group

4. Advanced Packaging

For Through-Silicon Via (TSV) seed layers in advanced interposers, continuous metal coverage of typical Ti-Cu to the bottom is mandatory for reliable Cu electroplating. It becomes challenging for standard sputtering to establish a conductive path for higher aspect ratios and via depths, whereas directional sputtering ensures full continuity. In more highly integrated devices, advanced packaging is becoming even more important.



SK Hynix HBM3 – HBM DRAM die: package cross section, SEM view



SK Hynix HBM3 – Bumps: package cross section, SEM view

Want to know more?

Got a challenging application? Want to investigate sampling opportunities in Evatec's Competence Laboratory (ECL)? Contact your local Evatec sales and service organization to find out more.

SEMICONDUCTOR & ADVANCED PACKAGING

FRONTEND

300mm frontend integration

Reaching for the sky

As the semiconductor industry evolves, it continues to follow two key innovation paths: “More Moore”, focusing on continued transistor scaling and performance improvements, and “More than Moore”, targeting functional diversification through advanced packaging and integration of different technologies.

Admir Asanoski, Head of Business Field Semiconductor and Advanced Packaging, and **Kai Wenz**, Senior Program Manager Technology Development, explain how Evatec supports both strategies with new innovative solutions.

The move to smaller feature sizes is relentless

With 2D scaling reaching physical limits, new strategies such as 3D integration, novel materials, and innovative device architectures are essential to meet the demands for higher logic density and multifunctional system performance. These trends demand increasingly sophisticated thin-film deposition capabilities, enhanced contamination control, and improved process reliability. Figure 1 illustrates the big picture where capabilities required for both strategies come together to satisfy increasingly complex device needs.

CLUSTERLINE® 300 – Building on a strong foundation

Evatec set the baseline back in 2022 for its initial planar frontend capabilities by having the right hardware in place through its CLUSTERLINE® 300 platform. Since that time we have been focused on an extensive program in advanced directional sputtering (ADS) to enable small feature sizes and more complex architectures. Figure 2 illustrates the principle of how we build a final solution optimized for mass production in the market combining hardware and process know-how.

We can already offer qualified processes for frontend planar layers like Ti, TiN, Al alloys, Ta and TaN at very low particle levels and layers free of metallic contamination. We can now also support next generation materials e.g. Ruthenium. We are continuing on our road of process development offering Standard Directional Sputtering (SDS) for lower aspect ratios (AR) up to 5:1 and via and trench structures with critical dimensions (CD) >110nm suplemented by Advanced Directional Sputtering (ADS) for higher performance and aspect ratios up to the limit of PVD for via and trenches CD >35nm.

A choice of

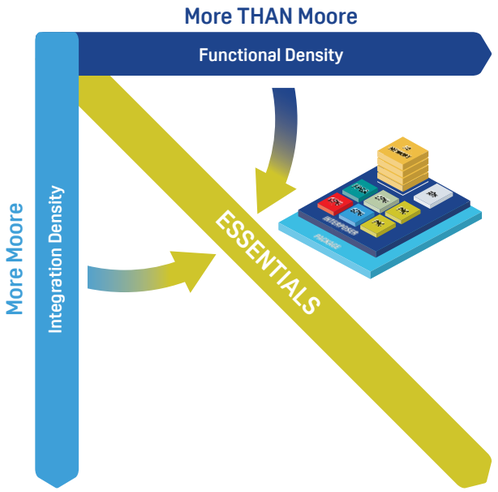


Figure 1: The Big Picture: Innovations for future essential chips.

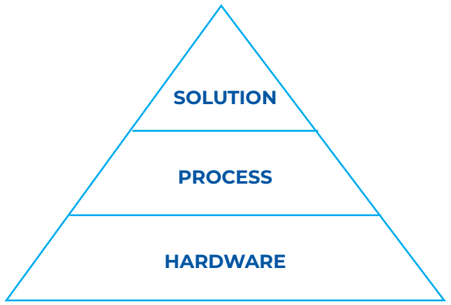


Figure 2: CLUSTERLINE® 300 – a strong foundation on which to build customer solutions.

Items	Conventional	High-End	
		Standard (SDS)	Advanced (ADS)
KEY FEATURES:			
HOT/COLD ESC			
SHUTTER			
			
WiW RS/THK uniformity	<5%	<3%	<3%
Target-Subtrate Distance	short	short /mid	long
Structures	Planar, Reflow	CD >110nm /AR 5:1	CD >35nm
Shutter	Yes	Yes	Yes
300mm hot/cold ESC	Yes	Yes	Yes
DC Sputter power	DC	DC	DC
	DC pulse	DC pulse	DC pulse
RF chuck bias	Yes	Yes	Yes

Figure 3: A range of solutions according to application demands.

CLUSTERLINE® 300 process modules

The current solutions available can be split into “conventional” and “high-end” frontend (see Figure 3). The conventional setup is focused on the best target utilization using long-life targets beneficial for thicker layers, whilst high-end solutions for thin layers are tuned for performance for each application.

In all cases, however, configurations are equipped with the same common capabilities such as shutters for cleaning and chamber preparation, hot/cold electrostatic chucks for full temperature control with full-face deposition, and supported by additional frontend reoptimized ICP etch chambers with H_2 capabilities, and high pressure degas and cool chambers.

Besides good WiW and WtW uniformity, the SDS solution can also deliver via nanostructures up to 5:1 AR with good step coverage performance (Figure 4). Further enhancement of performance will come with an ADS solution. Performance for trenches is typically even better by minimum factor of 1.5 compared to vias.

Mechanical particle levels can be controlled typically to levels in the range <20adders for sizes >60nm with metallic contamination controlled to <1.0E+10at/cm² for the standard frontend materials.

Productivity depends on the process flow. It can reach up to 50wph on a fully-equipped next generation CLUSTERLINE® 300 platform for TiAl deposition for memory applications. It achieves a barrier for Al through a 10nm thin Ti layer with excellent surface quality that avoids spiking into the silicon through full process control of our electrostatic chucks, pre- and post-treatments (Figure 5).

For different applications such as high bandwidth memory this Al layer can be temperature stress stable to achieve wafer bow always below <200µm.

We have in-house sampling capabilities for Ti, TiN, Al-alloys, Ta, TaN, and Cu including pre- and post-treatment like high pressure degas, cool, and ICP Etch (Ar and/or H_2). In-house metrology techniques include sheet resistance, thickness, particles, XRD, SEM /FIB, reflectivity (see Figure 6). Please also ask us about other materials for processing in basic and SDS module configuration.

There are many more exciting developments still to come on 300mm. Knowing that this is not the end, we already plan our next steps by adding the CVD and ALD capabilities that exist already on our 200mm platform to CLUSTERLINE® 300 too e.g. for high-end directional sputtering (HDS) and nanostructures <35nm where PVD on its own will no longer be sufficient. You can also read more about our ALD developments on page 26 in this year’s LAYERS.

The new developments for ADS and beyond will also include the development of a new cluster platform that will allow more single process chambers to be added to one platform fulfilling the solution needs that are planning to be released together with the final ADS solution. All these new developments will bring Evatec to the next level as a semiconductor solution provider, preparing for a future where we really can reach out for the sky together with our customers.

If you would like to learn more about what we are doing including accessing the capabilities within our ECL process laboratory, please “reach out” too! Simply contact your local Evatec service organization.

Structure dimensions	Diameter 110nm Depth 450nm	Diameter 160nm Depth 450nm	Diameter 250nm Depth 450nm
	Average %	Average %	Average %
Top Sidewall	19%	46%	43%
Middle Sidewall	10%	32%	27%
Low Sidewall	10%	33%	29%
Bottom	32%	17%	28%

Figure 4: SDS Step coverage performance.

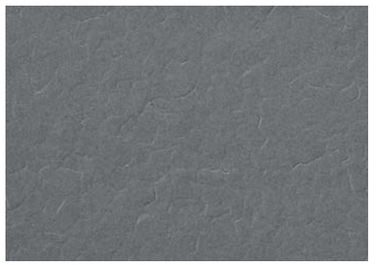
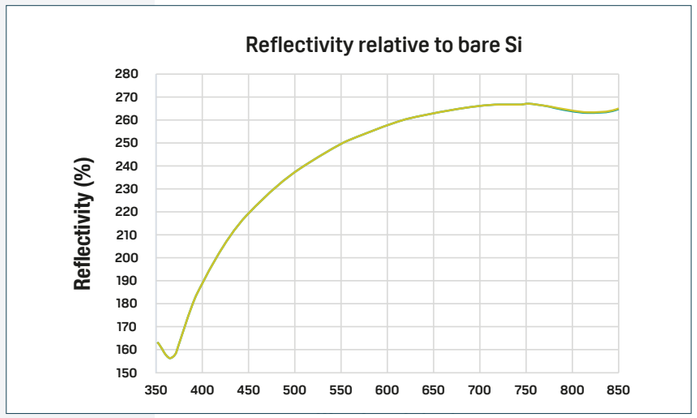


Figure 5: Excellent TiAl layer surface quality



Reflectivity refer to Si @436nm	Result
Center	212%
Edge	212%
Range	0.05%

Figure 6: Reflectivity performance of TiAl layer

Welcome to small panel processing – up to **310x310 mm!**

Since the launch of our first panel sputtering equipment in 2016, Evatec has become a leading supplier during early “take-up”. As the panel size has not really been standardized, our CLUSTERLINE® 600 has given high flexibility in this regard and can be configured based on the customer specific format going up to 650x650 mm. Our Head of Semiconductor & Advanced Packaging, **Admir Asanoski**, answers questions about the latest developments at Evatec when it comes to small panel processing for 300x300 mm or 310x310 mm.

01 What is driving the demand for 310x310 mm solutions?

In general, panel-level packaging (PLP) offers better material utilization than wafer-level packaging (WLP), leading to overall cost reductions regardless of size. The growing demand for smaller panels, such as 310x310 mm, is primarily driven by Artificial intelligence (AI) and high-performance computing (HPC) applications.

Smaller panels enable tighter control of critical dimensions and overlay accuracy, which is essential for these advanced applications. They also deliver higher yields thanks to reduced warpage, lower mechanical stress, and lower defect density compared to larger panels.

That said, demand for larger panel formats will continue to expand in parallel, particularly for mobile devices and next-generation IC substrate applications.

02 What experience do we already have for 310x310 mm solutions?

We are already delivering proven solutions for both 300x300 mm and 310x310 mm formats based on our CLUSTERLINE® 600 platform. Customers value that this equipment and the associated processes are well-established in production environments and can be easily adapted for smaller panel sizes.

Another key advantage is the panel size flexibility our system provides, a major factor in customers choosing this solution.

Looking ahead, we are exploring multi-panel handling capabilities that would enable processing of up to four small panels simultaneously, supporting customers as they scale their production capacity to the next level.

04 What's the approach to the new tool and what can customers expect?

In many ways, the new dedicated platform is primarily the result of an engineering effort rather than a new development project. It combines the proven strengths of our 12-inch wafer equipment "CLUSTERLINE® 300 & HEXAGON" and our panel system "CLUSTERLINE® 600", incorporating the necessary adaptations for the smaller panel size.

The system is built on our existing cluster wafer platform, ensuring the smallest possible footprint. This platform has already been production-proven in applications such as Backside Metallization (BSM) as a Thermal Interface Material (TIM) for heat dissipation, BSM / Frontside Metallization for power devices, optical coatings, and many other processes.

By integrating our established degas pre-treatment and Arctic Etch technology, customers can achieve rapid process integration for their specific small panel sizes while maintaining the same high performance and reliability as our existing systems.

This development marks an important milestone for Evatec, enabling customers to rely on a single source for both wafer and panel-level solutions. In addition to Ti/Cu RDL seed deposition, the new platform will also support our BSM / TIM process, featuring a highly efficient gold (Au) source that reduces target investment compared to conventional flat targets.

03 So why now develop a dedicated 310x310 mm tool?

While the CLUSTERLINE® 600 offers clear advantages and has proven its versatility in processing smaller panels, there are certain trade-offs that motivated the introduction of a dedicated small panel equipment.

Key drivers include footprint constraints, cleanroom cost considerations, and the need to optimize initial CAPEX investment for our customers.

This new tool will expand our panel-level product portfolio, providing customers with greater flexibility and the ability to select the system that best matches their production requirements and strategic goals.

05 How are you fast tracking the project?

To accelerate the engineering of the new system, we are leveraging our existing designs, proven technologies, and established supplier network. A strategy that ensures a fast time-to-market while maintaining the highest quality standards. Equally important, we are working closely with customers, involving them from the beginning, to ensure that all technical and operational requirements are met prior to delivery. A smooth installation and ramp-up phase is also an essential topic. This will be supported by our local Sales & Service Organizations (SSOs), who already have extensive experience with the existing platforms. In addition, we provide comprehensive customer training and on-site support (see article on page 12, LAYERS 9) from Evatec specialists to guarantee a seamless transition into high-volume production.

06 How can customers find out more about the tool and explore how it can meet their needs?

Customers can contact their local SSO for details on the tool, timelines, and how it fits their needs.

Advanced Packaging

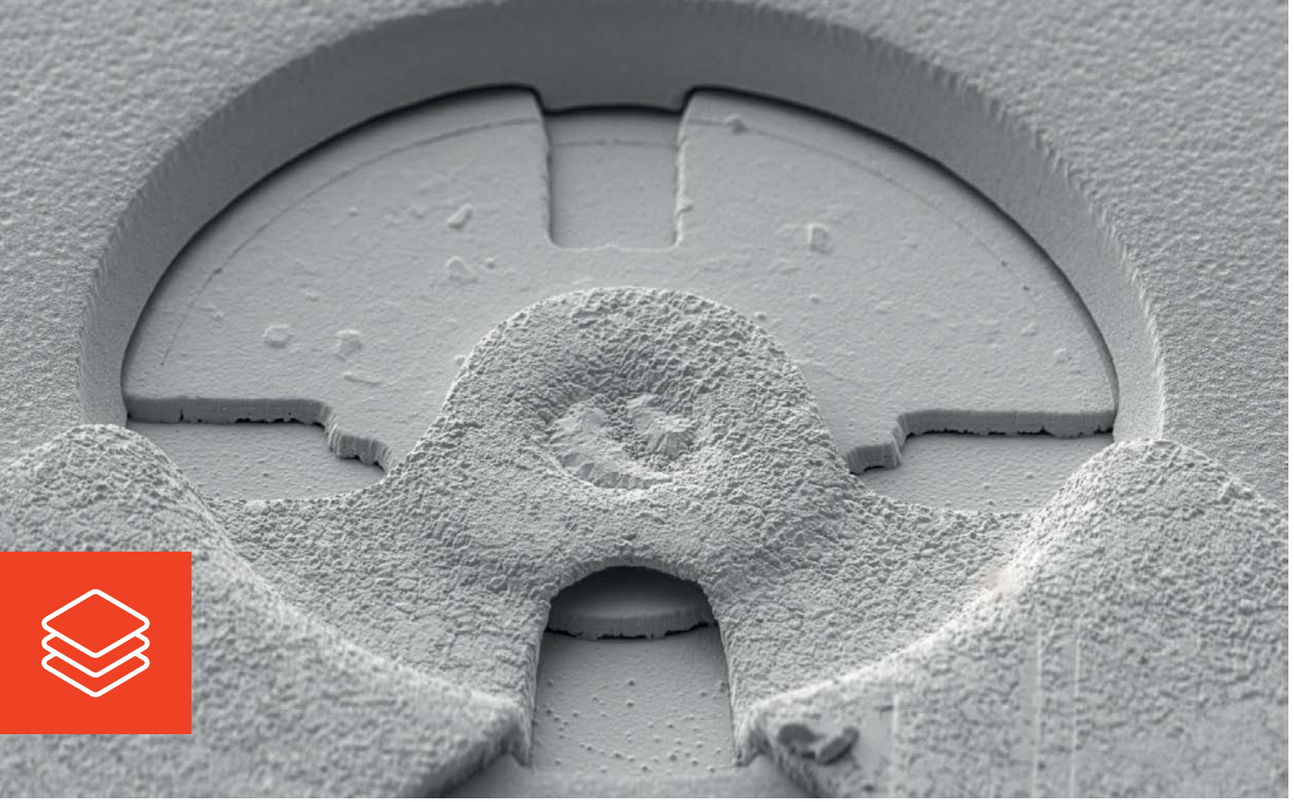
CLUSTERLINE® 600	HEXAGON	CLUSTERLINE® 300
		

Panel Level | **Wafer Level 300 mm**

Combining all strengths in one dedicated platform

EVATEC SOLUTION CLUSTERLINE® 310

- The base will remain and be used from our wafer equipment CLUSTERLINE® 300
- First application – RDL with 480 mm planar targets
- Second application – BSM with special source for Au



Development of a Highly Sensitive Test Vehicle for the Accurate Measurement of Seed Layer Contact Resistance in 2.0 µm-diameter Vias

Abstract

In the increasingly sophisticated semiconductor packaging landscape, multiple dies can be connected side-by-side on an interposer or stacked vertically to achieve shorter distances and higher interconnects density. These technologies allow the Heterogeneous Integration of chiplets with increased functionality, higher speed and better power efficiency. The high interconnects density and the concomitant shrinkage of the critical dimensions (e.g. RDL width/pitch and diameters of the vertical interconnections), increase exponentially the importance of the contact resistance between metal interfaces. In wafer-level packaging, interconnects are commonly manufactured by sputter deposition of a seed layer followed by Cu electroplating. The main challenge, prior PVD, is the elimination of the native oxide present on the exposed metal contacts, coupled with the presence of organic load released by the polymer dielectrics widely used in WLP (e.g. PI and PBO) that contaminates the process chambers of the PVD platform.

This work presents an improved wafer-level manufacturing process for fabricating Kelvin resistors based on Al/Ti/Cu metallization and via diameter ranging from 2.0 µm up to 20.0 µm. Experimental R_c data have shown that the sensitivity of the fabricated structures, in regard of the chamber conditions, is inversely proportional to the contact area. A test run of 25 wafers processed at a throughput of 55 wafers/hour on the HEXAGON has revealed a constant R_c on 10.0 and 20.0 µm via structures, but instead a significant excursion on the smaller vias. For example, 2.0 µm via structures exhibited R_c = 36.5 mΩ on wafer#1 and R_c = 44 mΩ on wafer#25. This corresponds to a 20% increase within lot. In conclusion, the fabricated Kelvin resistors are very suitable test vehicles to be used for benchmarking PVD seed layer processes and to establish optimum conditions ensuring high yield and a constant wafer-to-wafer quality in next-generation high-density interconnects WLP applications.

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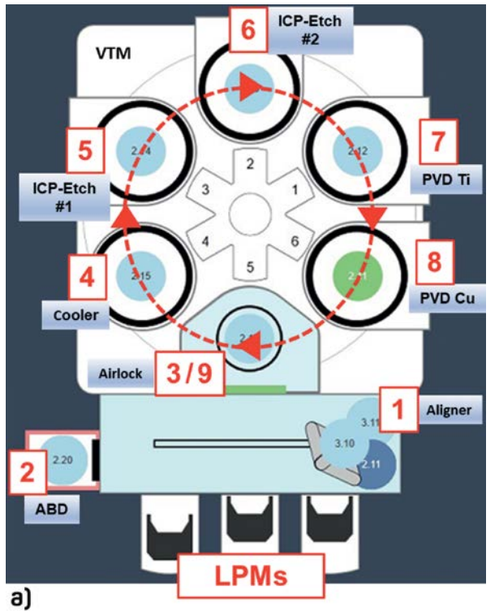
Introduction

The increasing demand for devices with higher speed and increased power efficiency, fueled by High-Performance Computing (HPC) and Artificial Intelligence (AI), is driving tremendous innovations in the electronics industry, both in frontend-of-line (FEOL), but even more in the field of advanced packaging [1]. TSMC's Chip-on-Wafer-on-Substrate (CoWoS) [2,3] and ASE's Fan-Out-Chip-on-Substrate (FOCoS) [4,5] are two examples of cutting-edge wafer-level packaging (WLP) technologies. Both combine multi-level fine-pitch redistribution layers (RDL) with shorter interconnect lengths and micro-bumps to enhance signal speed and power efficiency in 2.5D and 3D architectures. These technologies offer the advantage of a larger package size and more I/O connections per unit area. In addition, horizontal 2.5D and 3D stacking configurations of components enable the Heterogenous Integration of various processor and memory modules layer by layer, e.g. logic System-on-Chip (SoC) and High-bandwidth Memories (HBM) on the same IC platform [6,7].

Latest developments in advanced WLP applications often require RDL technologies with critical dimensions below 10 micrometers [8,9]. Therefore, a tight control of the contact resistance (R_c) is becoming increasingly important in high-volume manufacturing (HVM) to ensure high yield and a constant wafer-to-wafer quality. The smaller scaling of the interconnects is coupled with the presence of high loads of volatile contaminants released by the organic passivations widely used in WLP. The latter are typically spin-coated films of Polyimide (PI) or Polybenzoxaxole (PBO). State-of-the-art packaging platforms require the implementation of advanced strategies to mitigate the impact of hydrocarbon species and oxide contamination on the metal interfaces to avoid an adverse impact on R_c [10-13].

This work presents a wafer-level manufacturing process for the fabrication of Kelvin resistors based on the interface between a bottom Al electrode and an upper Ti/Cu metallization. A 5.0 µm-thick PBO passivation is present on the wafer, separating the two metallization levels, for mimicking the organic load of real WLP products. Various Kelvin structures with via diameter ranging from 2.0 to 20.0 µm have been designed. The smaller the via size, the higher the sensitivity of the structure in regard of process parameters and chamber conditions. The fabricated Kelvin resistors are suitable test vehicles to be used for monitoring the performance of the PVD process based on different throughput and conditioning frequency. The goal is to establish a set of optimum conditions that allow to keep low and stable R_c for a given via size at the highest throughput.

In a multi-level interconnects scheme, such as CoWoS and FOCoS, the PVD stack is present at numerous interfaces: (1) between the chip I/O's (i.e. Aluminum pads), and the first RDL, (2) between multi-level RDLs and (3) between the uppermost RDL and the under-bump metallization (UBM). The quality of these interfaces plays a fundamental role in the overall electrical device performance in terms of power consumption and signal integrity.



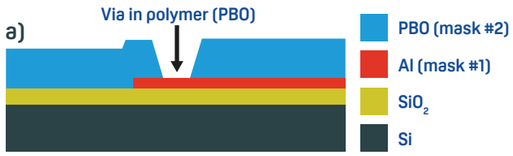
LPMs	
1	Aligner
2	Atm. Batch Degas

Figure 1:
a) State-of-the-art 300 mm HEXAGON used in high-volume manufacturing of wafer-level packaging,
b) Corresponding process flow that includes wafer pre-treatment steps and the deposition of adhesion and seed layers.

b)

In WLP, the adhesion/seed film stack is commonly deposited in state-of-the-art Cluster-type or Indexer-type multi-chamber PVD systems [14]. The wafer is pre-treated prior to the sputter deposition of the metal stack. First, degas is applied to drive out moisture from the organic passivation. This is followed by ICP sputter etch in Ar plasma to eliminate the native oxide from the exposed metal contacts. To ensure a low and stable R_c, especially at high throughputs, it is of utmost importance to mitigate the risk of re-contamination of the cleaned contacts by the volatile byproducts generated during the non-selective sputter etching of the wafer surface. The process strategy implemented on the Indexer platform has demonstrated best R_c control at the highest throughput achieved in HVM (Figure 1) [15]. The periodic conditioning of the ICP sputter etch chambers by "Aluminum pasting" is an integral part of the state-of-the-art process strategy implemented in the Indexer platform [10]. Pasting is an interruptive process that consists in the sputter etching of dedicated Al coated wafers, or bulk Al plates.

Keywords—Kelvin resistor, R_c, ICP sputter etch, PVD, seed layer, indexer, throughput



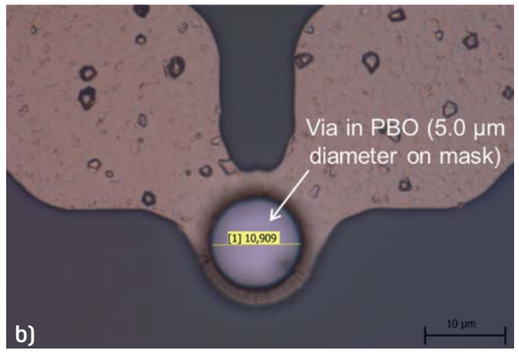
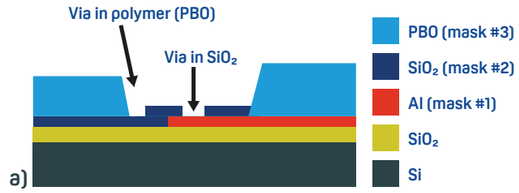


Figure 2: Fabrication process "Generation 1": a) schematic via cross-section before PVD seed layer, and b) top view of a via through PBO with 5.0 µm nominal diameter on mask. The measured opening is 10.9 µm.



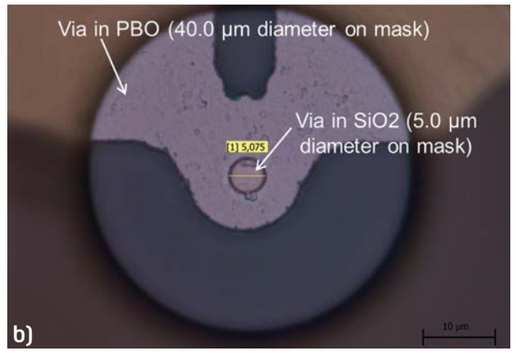


Figure 3: Fabrication process "Generation 2": a) schematic via cross-section before PVD seed layer, and b) top view of a 5.0 µm-diameter via through SiO_2 surrounded by a 40.0 µm-diameter via through PBO.

Al is a well-suited material for the pasting process due to its high chemical affinity towards volatile species, in particular oxygen, and its 50% higher sputtering rate in Ar plasma compared to SiO_2. Two main benefits are associated to the Al pasting process. These are the gettering effect on volatile contaminants, which can be measured by the rapid drop in the chamber base pressure, and the binding of solid residues onto the shields, that mitigates or delays the formation of particles. Generally, the first wafer processed after Al pasting benefits from best chamber conditions.

Experimental Method
Fabrication of Kelvin Resistors

In this work, Kelvin resistors are built on 300-mm Si wafers passivated with thermally grown oxide. As a first step, 1.0 µm-thick Al is sputter-deposited and patterned by reactive ion etching (RIE) to form the bottom electrode. Next a 5.0 µm-thick PBO passivation (HD-8820 from HD MicroSystems) is spin-coated and cured according to the temperature recommended by the supplier. A descum process in O2 plasma is carried out to remove PBO residues in the vias after the patterning by UV photolithography. In an earlier stage of our research, the mask-set referred as "Generation 1" was designed to include test structures with various via diameters ranging from 5.0 µm up to 30.0 µm. The fabricated vias systematically exhibited a tapered shape where the top opening exceeded the nominal diameter on the mask as shown in Figure 2a and 2b. A new mask-set has been designed and the corresponding fabrication process "Generation 2" has been established to overcome the resolution limitations of PBO photolithography in vias of aspect ratio (AR) = 1:1 and higher. The smaller the via diameter, the more sensitive the structure becomes in regards of the process parameters and chamber conditions.

Consequently, these new test vehicles allow to expand the R_c study towards more advanced interconnection schemes. To effectively achieve contact areas below 5.0 µm, a first set of vias is patterned by RIE into a 400 nm-thick PECVD SiO_2 film protecting the Al electrode (Figure 3a). Several design variations of round vias with diameter ranging from 2.0 µm up to 20.0 µm are present on the mask-set. The formation of SiO_2 vias is followed by PBO photolithography to open larger vias surrounding the previously formed ones. Beside the small contacts to the subjacent Al electrode, the PBO passivation layer on the wafer serves to mimic the organic load present on real WLP products. Figure 3b is a top view showing the two concentric vias: i.e. the 40.0 µm-diameter via in the PBO surrounding a 5.0 µm via patterned in the SiO_2 film.

Both in "Generation 1" and "Generation 2", after the formation of vias, the fabrication flow continues with the PVD seed layer process carried out on the Indexer platform (Figure 1). Here, the physical processes taking place include degassing at 120°C for 30 minutes, ICP sputter etch to remove a thickness of 30 nm equivalent to SiO_2, and finally, the sequential deposition of 100 nm of Ti and 200 nm of Cu. The downstream process continues with the formation of photoresist (PR) molds for the subsequent electroplating of a 3.0 µm-thick Cu film to reinforce the PVD seed layer. With an additional PR mask, Ni/Au electroplating is performed selectively on the four probing pads to provide a more reliable contact during probing. After electroplating, the PR layers are stripped and the Ti/Cu PVD films are wet-etched. As a last step, O2 plasma ashing is performed to remove any residues of seed layer left on the PBO surface that could potentially lead to shortcuts during the electrical characterization. The 25-wafers lot was processed on the Indexer system with the process-of-records resulting in a steady-state throughput of 55 wafers/hour.

There are differences in the number of total design variations and the base cell dimensions between mask-sets "Generation 1" and "Generation 2", but these are not relevant for the general description of the layout of the fabricated test structures. A 300-mm "Generation 1" test wafer (Figure 4a) contains approximately 750 base cells, each of these is constituted by an array of 11 x 11 = 121 structures (Figure 4b). Design variations include different via size and other parameters, e.g. the overlap width and access conductor width, that were investigated elsewhere [16]. Figure 4c is an enlargement of the base cell showing the layout of the fabricated 4-terminals Kelvin resistors. The size of the probing pads is ≈200 µm by ≈200 µm. Figure 4d is a zoomed view of the overlap area between the bottom Al electrode and Ti/Cu metallization with a 10.0 µm-diameter via in the center. Figure 4e shows a FIB cross-section of the contact area, revealing the tapered shape of the via formed in the PBO layer.

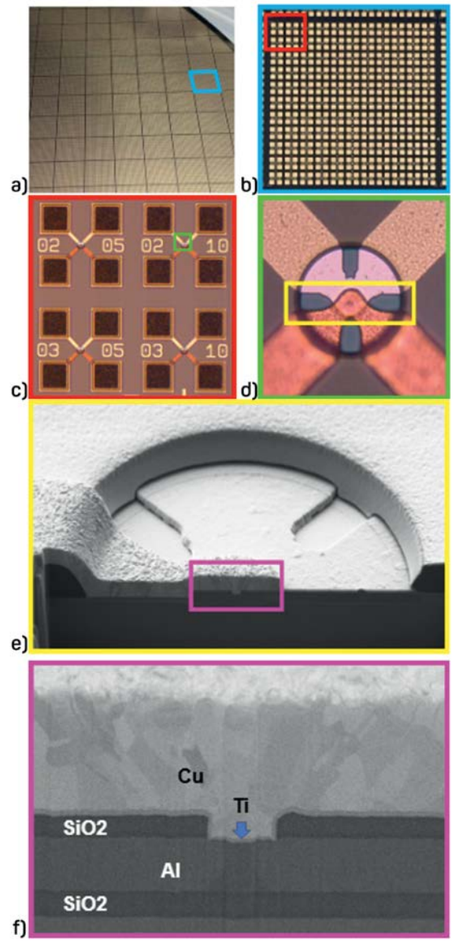


Figure 4: a) Fabricated 300 mm test wafer of "Generation 2", b) base cell containing an array of 11 x 11 Kelvin structures, c) example of Kelvin resistors layout, d) magnification of the contact area, e) FIB cross-section of the contact area of a 2.0 um-diameter via in SiO_2, and f) close-up of the interface between the underlying Al and the upper Ti/Cu metallization.

Electrical Characterization

The device characterization is performed at the wafer-scale using a vertical probe card. Four-points resistance measurement is conducted by forcing a current of 50.0 mA from terminal A to C, according to the sketch represented in Figure 5, and simultaneously measuring the potential difference between the opposite terminals B and D. The resistance of the Kelvin structure is calculated as the ratio of voltage divided by current: $R_K = V_{BD} / I$. In this study, R_K is considered as the contact resistance, R_c. However, an equivalent model has shown that R_K not only contains the R_c term, but also a geometrical factor, R_{GEOM} that accounts for 2-D current flow effects around the contact area [17]. Experimental data have shown that R_K increases when the overlap formed between the bottom and the upper metallization around the via becomes wider [16].

Contact Resistance Benchmark

The procedure to evaluate the stability of R_c in HVM-like conditions consists in placing electrical test wafers in slots #1, #13 and #25 of a 25-wafers lot, while the remaining slots are populated with PBO-coated dummies that mimic the outgassing load of real product wafers (Figure 6). In this study, the conditioning of the ICP sputter etch chambers by Al pasting is performed before the first wafer of the test lot.

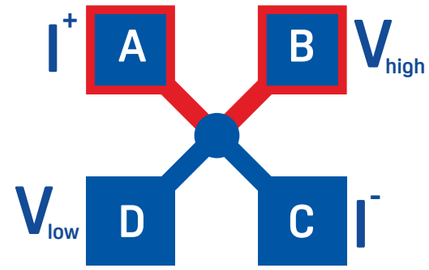


Figure. 5: Electrical characterization of 4-terminals Kelvin resistors.

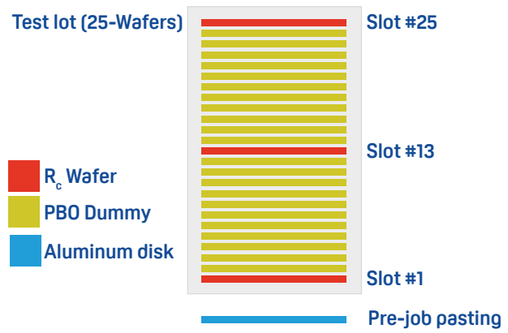


Figure 6: Procedure for the characterization of R_c stability within a 25-wafers lot. In this study, the ICP sputter etch chambers of HEXAGON are conditioned by Aluminum pasting prior processing the test lot.

Results

Figure 7a displays the R_c performance vs. via size obtained on structures of "Generation 2". As expected, R_c exhibits an increasing trend with the reduction of the via size. Structures with via diameter 20.0 µm show a R_c in the order of 3.0 mΩ, while structures with via diameter of 10.0 µm result in a R_c value of approximately 6.5 mΩ. In both cases, R_c remains constant within the lot. In contrast, a significant R_c trend-up can be observed on the smaller structures with via diameter ≤5.0 µm. The baseline of wafer#1 for the structures of via size 5.0 µm is ≈13 mΩ. This increases by 11% on wafer#25. The baseline of wafer#1 for via size 3.0 µm is ≈22 mΩ. Here, the increase within lot is 19%. Finally, the 2.0 µm via structures of wafer#1 exhibit a R_c of ≈36.5 mΩ and ≈44 mΩ on wafer#25, corresponding to an increase of 20%. Beside the geometrical factor predicting higher R_c for structures with smaller vias, the latter also exhibit a higher trend-up within the lot. Clearly, the accumulated contamination in the chamber during continuous wafer run has a more detrimental effect on the vias ≤5.0 µm.

Ho et al. reported R_c values of ≈20.0 mΩ measured on Kelvin resistors built with Cu/Ti/Cu metallization and a 2.4 µm-diameter via in 5.0 µm-thick polymer [9]. Our previous research has also demonstrated that the contact resistance measured on Cu/Ti/Cu interfaces is generally lower than the value measured on Al/Ti/Cu structures with same geometry [18].

Figure 7b compares side-by-side the R_c datasets of Kelvin resistors of "Generation 2" and "Generation 1" with 5.0 µm vias. Structures of "Generation 1" exhibit a lower R_c baseline and a larger data spread compared to "Generation 2". The inspection of the fabricated structures of "Generation 1" has revealed that the vias patterned in 5.0 µm-thick PBO have a tapered shape with a 50% enlargement of the opening at the top compared to the mask design (see Figure 2b).

This enlargement is caused by limitations of the photolithography resolution and very likely also by the step of plasma ashing after photolithography. The larger experimental spread may also indicate that the contact area is not constant over the entire wafer surface. On the other hand, structures of "Generation 2" reveal via openings in the SiO_2 passivation that are identical to the mask design (see Figure 3b). A narrower R_c spread is desirable as it allows for a more reliable benchmark between different process conditions.

Conclusion

A novel wafer-level manufacturing process has been developed to build Kelvin resistors with miniaturized via sizes. The approach consists in first patterning a via into a 400 nm-thick SiO_2 passivation covering a bottom Al electrode. This is followed by the patterning of a larger via surrounding the first one, in a 5.0 µm-thick spin-coated PBO passivation. The fabrication process is completed by the patterning of a Ti/Cu upper metallization. To our best knowledge, this work reports for the first time R_c data measured on Kelvin resistors with via size as small as 2.0 µm on Al/Ti/Cu contacts.

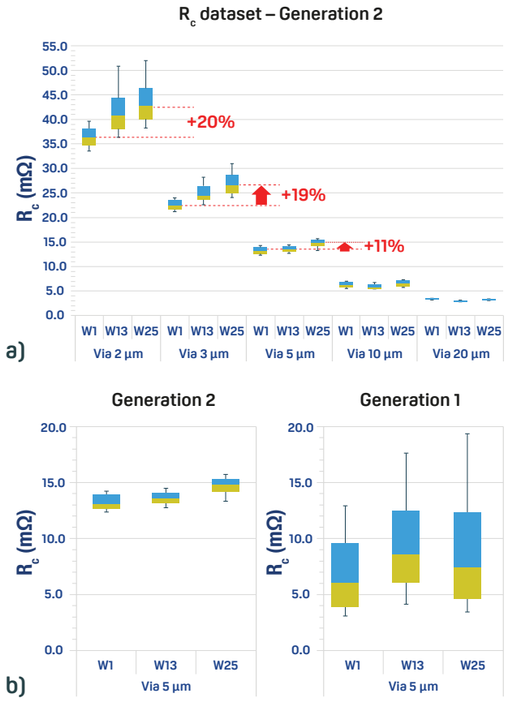


Figure. 7: a) R_c performance vs. via diameter and wafer position for Kelvin resistors fabricated with the improved process "Generation 2", and b) comparison of R_c obtained on 5.0 µm via structures of "Generation 1" and "Generation 2".

Experimental data has demonstrated that the process-of-records executed on the HEXAGON at a throughput of 55 wafers/hour and Al pasting performed before the test lot, delivers low and stable contact resistance in structures with via diameters of 10.0 and 20.0 µm.

In contrast, an excursion of R_c within lot can be observed on structures with via size ≤5.0 µm. This can be attributed to the accumulated load of volatile contaminants especially in the ICP etch chambers during continuous run at throughput of 55 wafers/hour and indicates excellent sensitivity of Kelvin resistors of "Generation 2" in regard of the process environment. Therefore, these test vehicles are suitable for optimizing PVD seed layer process conditions in HVM of current and next-generation high-density interconnects WLP applications.

Future work will include the optimization of the Aluminum pasting frequency allowing to keep R_c stable within lot, especially at peak throughputs above 90 wafers/hour that can be reached on the HEXAGON.

Acknowledgments

The authors would like to acknowledge Nico Härtl at Evatec Ltd. for support in wafer processing activities.

References

1. *J. H. Lau, "Recent Advances and Trends in Advanced Packaging", IEEE Trans. Components, Packaging and Manufacturing Technology, Vol. 12, No. 2, Feb. 2022, pp. 228-252.*
2. *P. K. Huang et al., "Wafer Level System Integration of the Fifth Generation CoWoS®-S with High Performance Si Interposer at 2500 mm2", IEEE 71st Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2021, pp. 101-104.*
3. *Y.-H. Hu et al., "CoWoS Architecture Evolution for Next Generation HPC on 2.5D System in Package", IEEE 73rd Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2023, pp. 1022-1026.*
4. *J.-K. Fang, M.-L. Huang, H.-J. Tu, W.-L. Lu, and P. Yang, "A Production-worthy Fan-Out Solution – ASE FOCoS Chip Last", IEEE 70th Electronic Components and Technology Conference (ECTC), 2020, pp. 290-295.*
5. *W. Wudjud et al., "Advanced Thermocompression Bonding on High Density Fan-Out Embedded Bridge Technology for HPC/AI/ML Applications", IEEE 74th Electronic Components and Technology Conference (ECTC), Denver, CO, USA, 2024, pp. 929-935.*
6. *J. H. Lau, "Recent Advanced and Trends in Heterogeneous Integration", J. Microelectronics and Electronic Packaging, Vol. 16, 2019, pp. 45-77.*
7. *S. Zhang et al., "Challenges and Recent Prospectives of 3D Heterogeneous Integration", e-Prime – Advances in Electrical Engineering, Electronics and Energy, 2022 (2), pp 1-14.*
8. *A. Kubo et al., "Reliability Studies of 5 µm Diameter Photo Vias with Daisy Chain Resistance using Dry Film Photosensitive Dielectric Material", IEEE 68th Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2018, pp. 1556-1560.*
9. *S. W. Ho et al., "Polymer-based Fine Pitch Cu RDL to Enable Cost-effective Re-routing for 2.5D Interposer and 3D-IC", IEEE 15th Electronics Packaging Technology Conference (EPTC), Singapore, 2013, pp. 435-439.*
10. *P. Carazzetti et al., "Impact of Process Control on UBM/RDL Contact Resistance for Next-Generation Fan-Out Devices", IEEE 67th Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2017, pp. 909-916.*
11. *P. Lianto et al., "Under-Bump Metallization Contact Resistance (R_c) Characterization at 10-µm Polymer Passivation Opening", IEEE Trans. Components, Packaging and Manufacturing Technology, Vol. 7, No. 10, Oct. 2017, pp. 1592-1597.*
12. *A. Barker et al., "Understanding and Improving R_c management for Wafer Level Packaging through Novel PVD Processing", IEEE 26th Electronics Packaging Technology Conference (EPTC), Singapore, 2024, pp. 238-242.*
13. *K. Zhang et al., "Advanced Preclean Chamber for UBM/RDL Contact Resistance Improvement in Advanced Node Packaging Application", Proc. 17th Int. Wafer Level Packaging Conference (IWLPC), San Jose, CA, USA, 2020.*
14. *P. Carazzetti et al., "Study of Cross-Contamination in Multi-Chamber PVD Systems Used for High-Throughput Seed Layer Deposition", IEEE 10th Electronics System-Integration Technology Conference (ESTC), Berlin, Germany, 2024.*
15. *C. Drechsel et al., "Optimum R_c Control and Productivity Boost in Wafer-Level Packaging Enabled by High-Throughput UBM/RDL Technology", IEEE 73rd Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2023, pp. 126-131.*
16. *P. Carazzetti et al., "Investigation of UBM/RDL Contact Resistance Based on ICP Sputter Etch Conditions and Critical Design Dimensions", IEEE 26th Electronics Packaging Technology Conference (EPTC), Singapore, 2024, pp. 320-325.*
17. *N. Stavitski, J. H. Klootwijk, H. W. van Zeijl, A. Y. Kovalgin, and R. A. M. Wolters, "Cross-Bridge Kelvin Resistor Structures for Reliable Measurement of Low Contact Resistances and Contact Interface Characterization", IEEE Trans. on Semiconductor Manufacturing, Vol. 22 (1), Feb. 2009, pp. 146-152.*
18. *P. Carazzetti, J. Weichart, A. Erhart, M. Elghazzali, and E. Strolz, "Evaluation of ICP Sputter Etch with Reducing Atmosphere for the Improvement of R_c in UBM/RDL Applications", IEEE 70th Electronic Components and Technology Conference (ECTC), 2020, pp. 1711-1717.*

Enabling Robust SiC Power Device Fabrication with **Amorphous-Carbon Sputtering**

Evatec's Manager Process Development, **Gerald Feistritzer**, and Business & Technology Scouting Manager, **Dr. Vinoth Sundaramoorthy**, explain the motivation for using PVD processes for amorphous carbon (a-carbon) cap layers as a superior alternative to typical photoresist processes and report results for processes developed on CLUSTERLINE® 200. In addition to post-doping PVD deposition, a novel approach to pre-doping PVD deposition of the a-carbon layer was shown to be a potentially useful technique to modify the doping profile and downstream device performance.

Why Cap layers?

Silicon Carbide (SiC) materials have a wide band gap and high thermal conductivity compared to silicon materials, which makes them suitable in high-voltage applications. They can also be used for harsh environments (automotive, aerospace) where robustness and reliability of the semiconductor device are crucial. It is not easy to dope these materials using "diffusion", so they are typically "implanted" with high doses and at high energies to achieve source and drain regions of the silicon carbide power device.

Post-implantation annealing is then required to activate the dopants during SiC device fabrication, as the implanted dopants lie deep inside the bandgap. Annealing temperatures typically higher than 1600°C are used for dopant activation. During such high-temperature annealing, the surface of SiC substrates becomes very rough due to the out-diffusion of carbon atoms. This process, called "step bunching", causes surface degradation and affects the performance of the devices fabricated on these layers. In particular, the Metal-Oxide-Semiconductor (MOS) interface fabricated on these layers poses severe reliability issues. Hence, it is important to protect the SiC surface during the dopant activation annealing process.

Improving on existing CVD solutions

A thick carbon layer formed by depositing photoresist and annealing above 800 °C is typically used as surface protection during such a high-temperature activation process. However, this approach is not ideal for mass production with respect to both cleanliness and particle management, which might lead to yield issues in the fabricated devices. We have now been able to demonstrate that sputtering can serve as an effective alternative for the surface protection layer for SiC wafers.

Device Structure	Planar	Trench
Target - Substrate Distance	50mm	125mm
Typical film thickness (nm)	20 - 200	
WiW uniformity (%)	<5%	<15%
Typical deposition rate (nm/s)	1.5 - 1.7	0.6 - 0.8
Refractice index	2.3 - 2.4	
Typical film stress (MPa)	-800 to -400	

Figure 1a: Process performance data

- → System configuration: Single Process Modules (SPM)
- → Vacuum system: Cryo-pump
- → 6” or 8” chuck at room temperature
- → Shadow mask (full face deposition)
- → ARQ 151 DC sputtering 6kW, Ar sputter gas
- → Carbon target
- → Zoom shield

Figure 1b: Hardware configuration

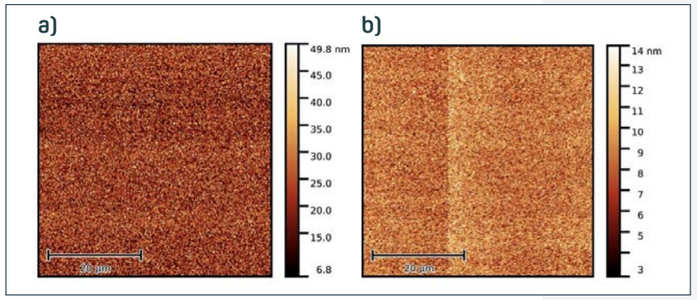


Figure 2: AFM analysis on samples with a) 20nm, b) 50 nm a-carbon layer. Both samples were annealed at 1800 °C.

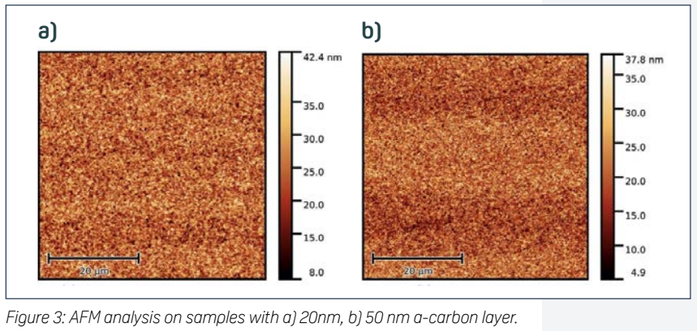


Figure 3: AFM analysis on samples with a) 20nm, b) 50 nm a-carbon layer. Both samples were annealed at 1900 °C.

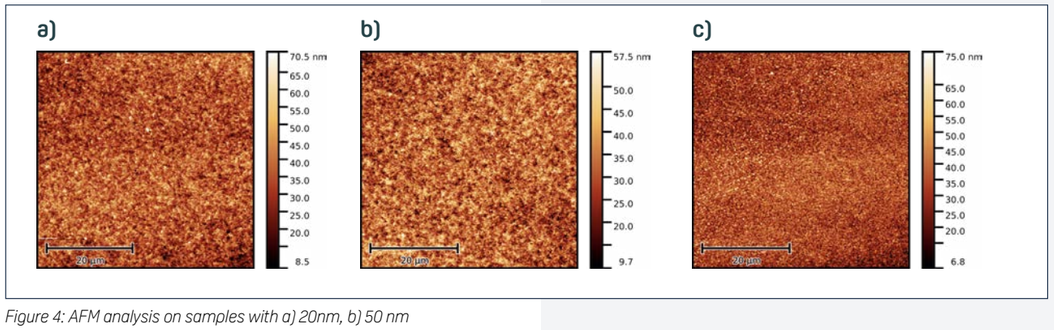


Figure 4: AFM analysis on samples with a) 20nm, b) 50 nm c) 280 nm a-carbon layer. All samples were annealed at 2000 °C.

Figures 2, 3, 4, 5 & 6 courtesy of Fondazione Bruno Kessler, Italy

PVD solutions on CLUSTERLINE® 200

Evatec’s advanced amorphous-carbon sputtering solution is specifically engineered for planar and trench power device applications. It enables high quality deposition using a single process module, streamlining production while ensuring exceptional uniformity and repeatability.
The hardware configuration, detailed in Figure 1b, delivers both flexibility and precision for demanding power device manufacturing environments.

Process results

To demonstrate the surface protection capability, a range of amorphous carbon layers were coated onto 6” 4H n-type SiC substrates with a thickness of 350 µm and a resistivity of 0.02Ωcm. The a-carbon layers were deposited using typical deposition conditions shown in Figure 1a.

Two thicknesses of amorphous-carbon layers were selected for the experiments: 20 nm and 50 nm. For comparison, a wafer with a carbon layer formed by photoresist and annealing was also analyzed. The wafers were annealed in a centrotherm c.ACTIVATOR 200 furnace at temperatures between 1800°C and 2000°C. To benchmark the performance of the photoresist-formed carbon layer, an equivalent thickness (280 nm) of PVD a-carbon layer was also deposited on SiC wafers. Finally, structural analysis was performed at partner Fondazione Bruno Kessler (FBK) in Italy.

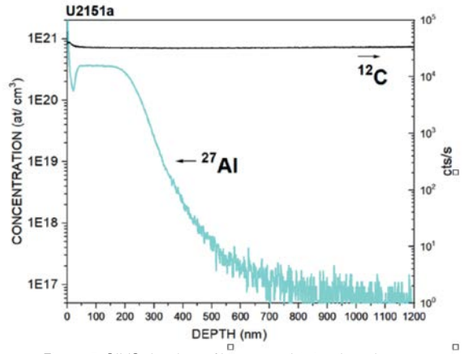


Figure 5: SIMS depth profiles were obtained on the sample implanted with Al species at 500°C. A 50 nm a-carbon layer was deposited before implantation.

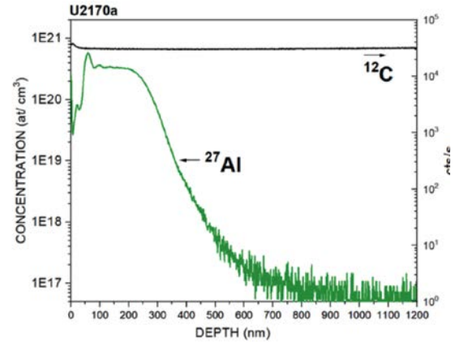


Figure 6: SIMS depth profiles were obtained on the sample implanted with Al species at 500°C. A 50 nm a-carbon layer was deposited after implantation.

	Temperature		
A-Carbon thickness (nm)	**1800°C**	**1900°C**	**2000°C**
20 nm	4.46 ± 0.42 nm	4.32 ± 0.26 nm	6.61 ± 0.53 nm
50 nm	2.12 ± 0.19 nm	4.18 ± 0.32 nm	6.49 ± 0.48 nm
280 nm	–	–	6.15 ± 0.47 nm

Table 1: Comparison of surface roughness for different a-carbon layer thickness until 2000°C annealing temperatures.

In Figures 2 and 3, we can see that sputtered PVD layers provide good protection of SiC surfaces up to 1900°C with a minimum layer thickness of 20 nm. It was also seen that the surface roughness decreases for SiC wafers with increasing amorphous-carbon protection layer thickness until 2000°C. For temperatures of 2000°C (Figure 4), 20 nm thick layers are not sufficient, but the properties improve with increasing layer thickness. The values of the surface roughness measured using Atomic Force Microscopy (AFM) are recorded in Table 1. It can be seen that the average surface roughness of the SiC surface decreases with increasing a-carbon layer thickness at all annealing temperatures until 2000°C. In general, a 50 nm a-carbon layer can protect the SiC surface against step-bunching until 1900°C, comparable with the performance of a-carbon layer formed from photoresist, and this is a very useful feature for making novel semiconductor devices like super-junction structures.

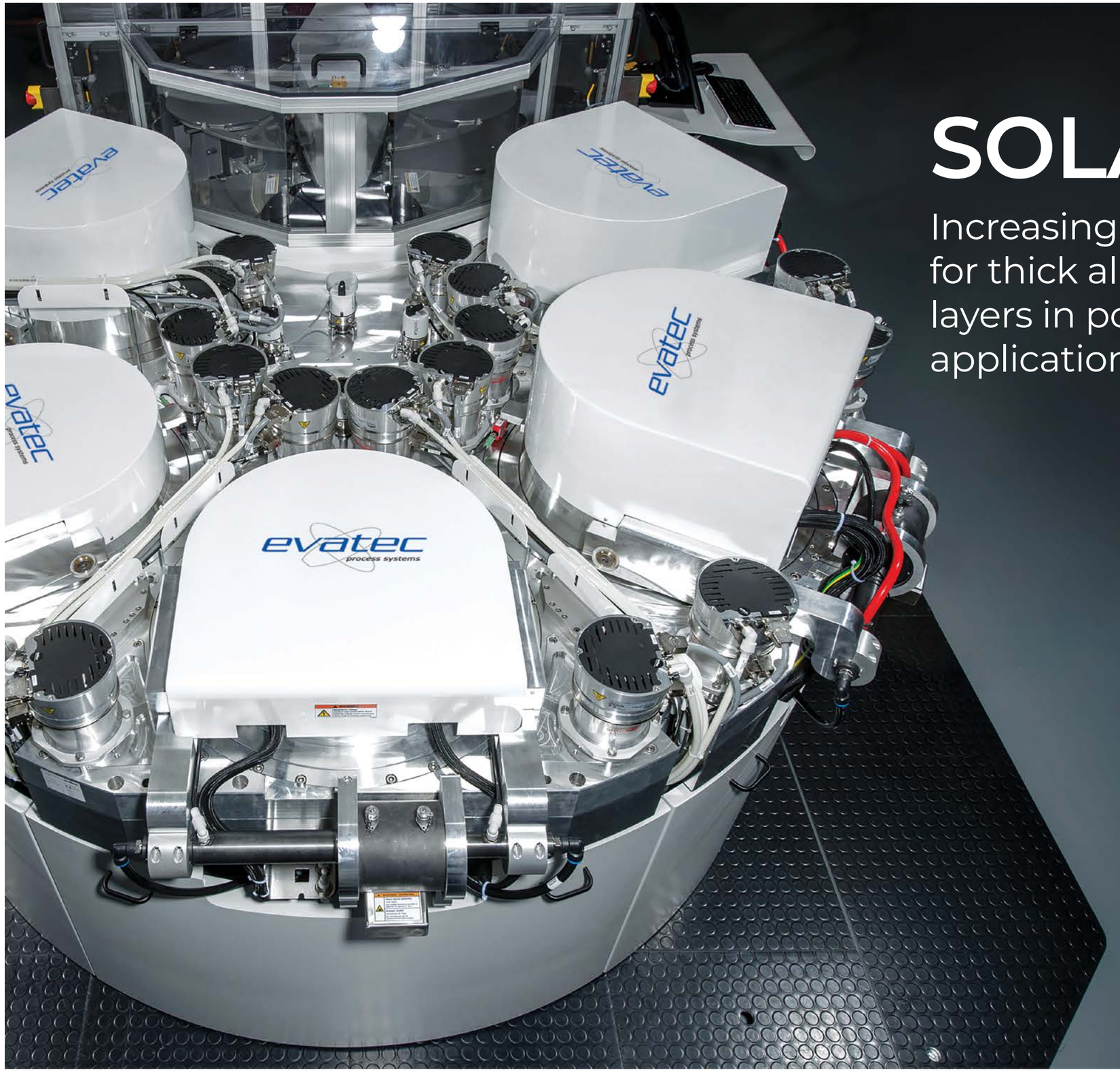
Modification of dopant profile in SiC layers

A-carbon was analyzed as a surface protection layer on the implanted samples to test its effectiveness in screening the defects that are generated during the implantation process. SiC wafers were implanted with Al or P species at different doses and energies to create a dopant profile. Again, two different a-carbon layers were deposited: 20 nm and 50 nm. An a-carbon layer was deposited on some wafers before implantation and some wafers after implantation to analyze the screening effectiveness. All implanted samples were annealed at 1750°C. SIMS profiles were performed on these implanted wafers to investigate the effectiveness of the a-carbon layer.

It can be seen from Figure 5 that a 50 nm a-carbon layer deposited before the implantation avoided the spike in carrier concentration on the surface of the SiC wafer. The peak carrier concentration of Al was 3.5E20 cm^{-3}.

Similarly, the peak carrier concentration of Al in the sample where a 50 nm a-carbon layer was deposited after the implantation process was 6E20 cm^{-3}, which was observed as a spike in the Al concentration (Figure 6). Hence, the doping profile of the implanted wafers can be altered with a thin a-carbon layer. This could be due to the fact that the a-carbon layer acts as screening layer in blocking peak concentration on the SiC surface and reduces the defects formed on SiC surface during the implantation process. This feature could be very helpful in modifying the implant profile and modulating the device performance.

These results enable novel design and support chip manufacturers to produce next generation SiC devices. Let’s talk some more about how we can support you and your own process innovations.

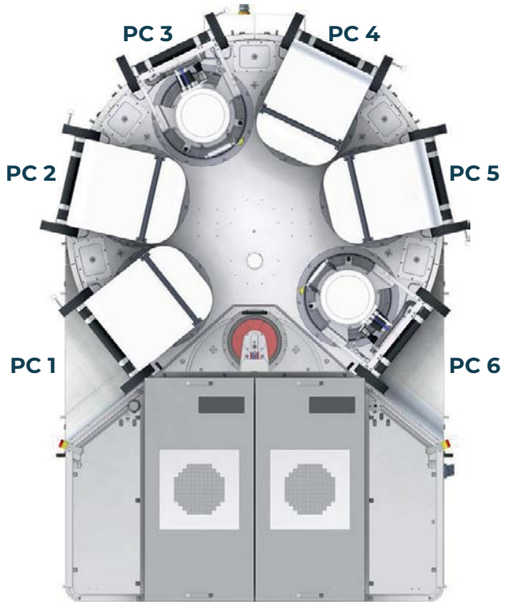


SOLARIS®

Increasing throughput for thick aluminum layers in power device applications

Evatec's Manager Process Development, **Gerald Feistritzer**, shows us how SOLARIS® is proving itself as a valuable addition to Evatec's armoury of thin film production tools in power device applications.

Evatec has a long history of delivering metallization production solutions using both evaporation and sputter process technologies. For many customers and process steps including "lift-off", evaporation remains the technology of choice. For others where fab integration requirements call for elimination of manual wafer handling, cassette-to-cassette processing offers the potential to improve throughput if handling times relative to classical cluster tools can be driven down. In addition, wafer breakage through operator errors can also be reduced, increasing overall process yield. In this article we report on studies to investigate how the SOLARIS® could deliver the thick Al layer performance required with a boost to process throughput.



PC 1, 2, 4 & 5 ARQ 151 Target: Al
PC 3 & 6 Cooling Station CS21 Cooler: Julabo FP51

Figure 1: SOLARIS® S151 configuration for thick Al (4x ARQ151 for Al & 2x cooling station)

Simulations

We knew that the unique handling approach of parallel carrier transfer around SOLARIS® S151 by synchronous indexer was the perfect basis to achieve high speed processing of 8 inch substrates. We would need to meet customers process requirements of sputtering thick Al films (typicaly 1 – 18 µm) on both front and backside of their devices without exceeding typical temperature limits of around 300°C.

Temperature simulations were performed as a first step to define the optimum hardware configuration showing that a SOLARIS® with 4 PVD and 2 cooling chambers would be the best choice.

The process would then consist of Al sputtering in two consecutive chambers until the temperature limit was reached, followed by a cooling step where the substrate temperature would fall back towards room temperature.

With the proposed configuration, we established that two such process sequences could be incorporated in one complete rotation of the indexer. Figures 2 and 3 show two examples, where either 1000nm or 1250nm can be deposited in such a cycle. The process power for this simulation is 13kW.

The design of the SOLARIS® allows for thicker layers to be coated simply by making multiple cycles. This calculation also assumes that seven substrates are always in the tool at the same time (six PVD chambers and one load-lock). We derived a theoretical throughput of almost 60 wafers/hour for 2µm thick Al layers and more than 16 wafers/hour for layers of 18µm (Figures 4 & 5).

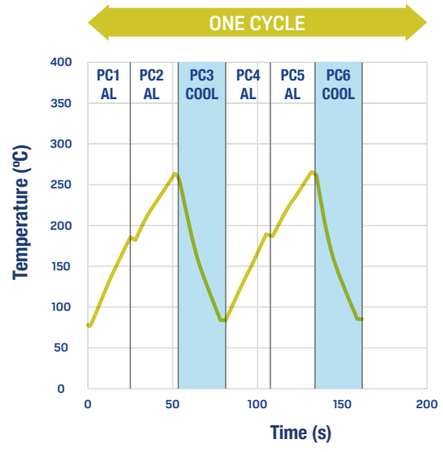


Figure 2: Simulation of substrate temperature for one cycle with 2xAl 500nm / 1x cooling / 2xAl 500nm/1x cooling.

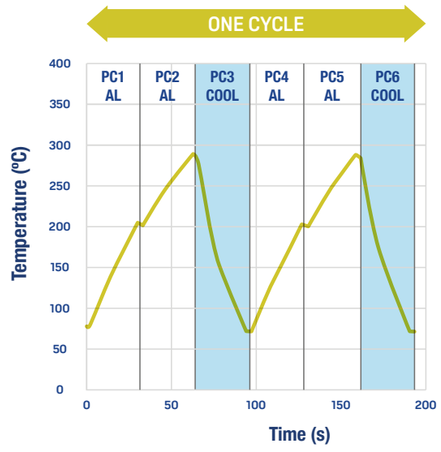


Figure 3: Simulation of substrate temperature for one cycle with 2xAl 625nm / 1x cooling / 2xAl 625nm/1x cooling.

Experimental results

Figure 6 illustrating the uniformity measurement of the sheet resistance of an 18µm thick Al layer on a 6" Si substrate shows acceptable results. In Figure 7 we also then see a comparison of the theoretical throughput values between BAK and SOLARIS® with two different domes showing the gains using SOLARIS®.

The benefits are clear

From these studies we see that SOLARIS® could deliver a significant throughput advantage relative to a BAK when transitioning from 6-inch to 8-inch wafers. With its fully automated cassette-to-cassette solution, and flexible carrier concept changing between substrate sizes is easy. The tool enables clean, reliable, and scalable production of double-sided processes with integrated flipper and a reduced layout, perfectly suited for modern manufacturing demands.

	PC1	PC2	PC3	PC4	PC5	PC6
Process	DC	DC	Cooler	DC	DC	Cooler
Material	Al	Al	n/a	Al	Al	n/a
Sputter rate [nm/s]	21.45	21.45	n/a	21.45	21.45	n/a
Thickness [nm]	625	625	0	625	625	0
Process time [si	29.14	29.14	29.00	29.14	29.14	29.00
Uptime [%]	100					
Cycles	2.00					
Cycle time [s]	30.54					
Throughput Wafer/hour	58.94					

Figure 4: Throughput calculation for 2.0um Al with 13kW sputter power.

	PC1	PC2	PC3	PC4	PC5	PC6
Process	DC	DC	Cooler	DC	DC	Cooler
Material	Al	Al	n/a	Al	Al	n/a
Sputter rate [nm/s]	21.45	21.45	n/a	21.45	21.45	n/a
Thickness [nm]	500	500	0	500	500	0
Process time [si	23.31	23.31	23.00	23.31	23.31	23.00
Uptime [%]	100					
Cycles	9.00					
Cycle time [s]	24.71					
Throughput Wafer/hour	16.19					

Figure 5: Throughput calculation for 18.0um Al with 13kW sputter power.

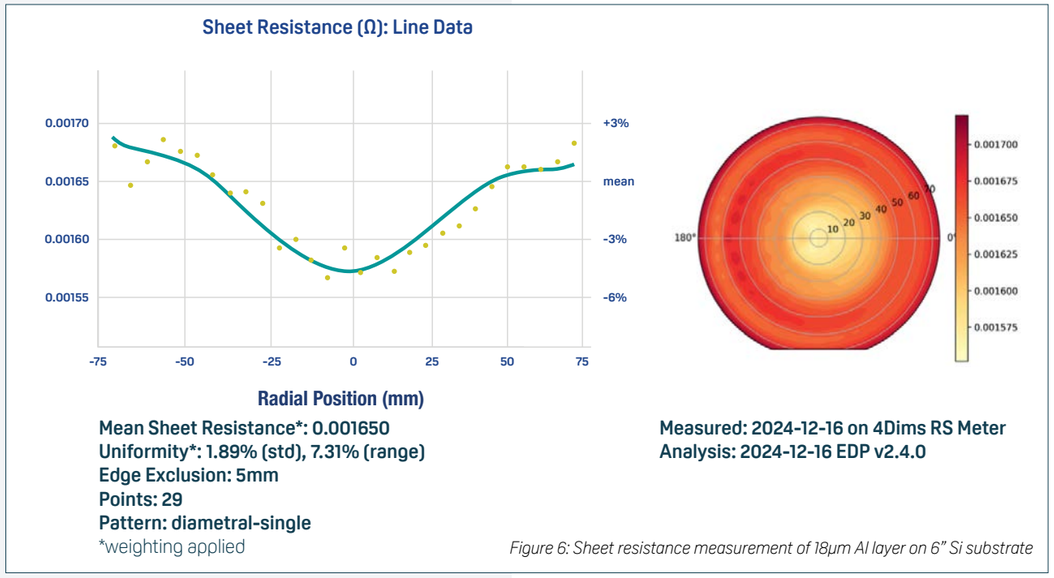


Figure 6: Sheet resistance measurement of 18µm Al layer on 6" Si substrate

		BAK 761 (Knudsen)	BAK 1401 Split Chamber (Dome calotte)	SOLARIS®
Thickness (µm)	Wafer size	Throughput (wph)		
2.0	6"	30.3	34.4	58.9
	8"	12.6	19.6	58.9
18.0	6"	11.8	7.1	16.2
	8"	4.9	4.1	16.2

Figure 7: Comparison of theoretical throughput values (wafers per hour) between BAK and SOLARIS® for 2.0 and 18µm Al coatings.

Powering the SiC Future

How Evatec's CLUSTERLINE® 200 empowers next generation MOSFETs

Dr. Yuan Lu, Evatec China's Manager of Technical Marketing Management, shares how the CLUSTERLINE® 200 is empowering customers in 200 mm SiC power MOSFET production through a proven platform and local service support.

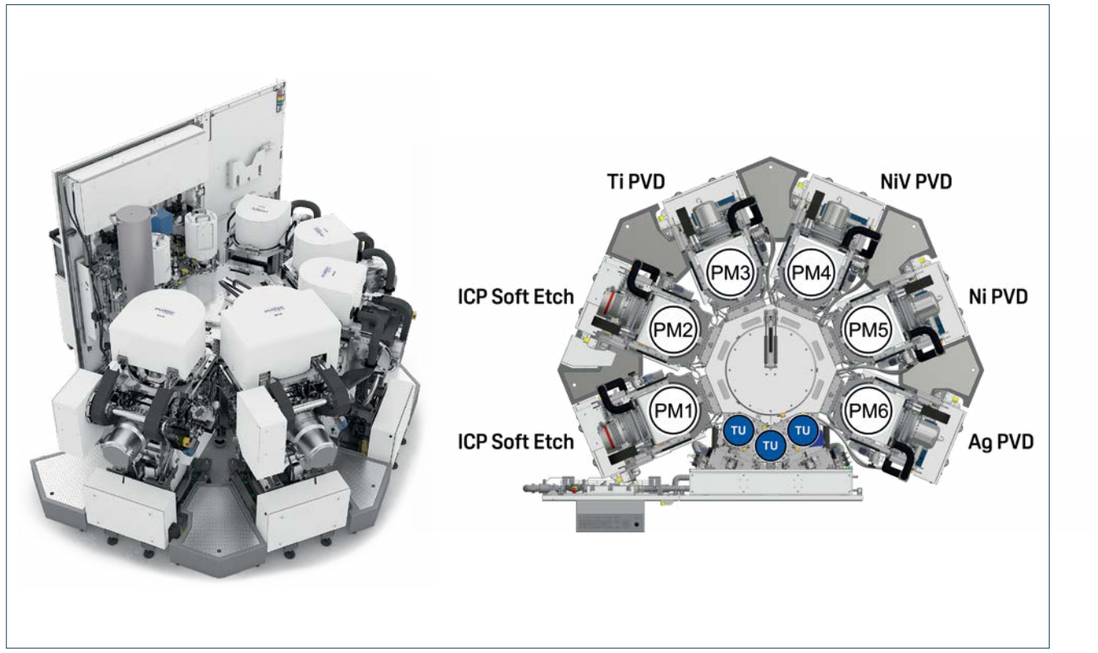


Figure 1. Left: CLUSTERLINE® 200 Platform.
Right: Configuration of CLUSTERLINE® 200, equipped with 6 SPM with 6 TU modules, perfect for BSM, STM and Silicide.

Silicon Carbide (SiC) has become a strategic enabler for the transition to high-efficiency power electronics, with SiC MOSFETs driving advances in electric vehicles (EVs), renewable energy, and industrial power systems. Compared with traditional silicon devices, SiC MOSFETs deliver lower switching losses, higher breakdown voltage, and superior thermal performance.

The domestic EV industry in Asia is the primary driver, and demand is forecast to keep expanding at double-digit rates. SiC MOSFETs are increasingly integrated into traction inverters, onboard chargers, and DC/DC converters to extend range and enable fast charging. To meet this demand, global leaders and local players are investing heavily in Asia. STMicroelectronics, Infineon, and Wolfspeed have partnered with local foundries and assembly houses to accelerate SiC adoption in the EV supply chain.

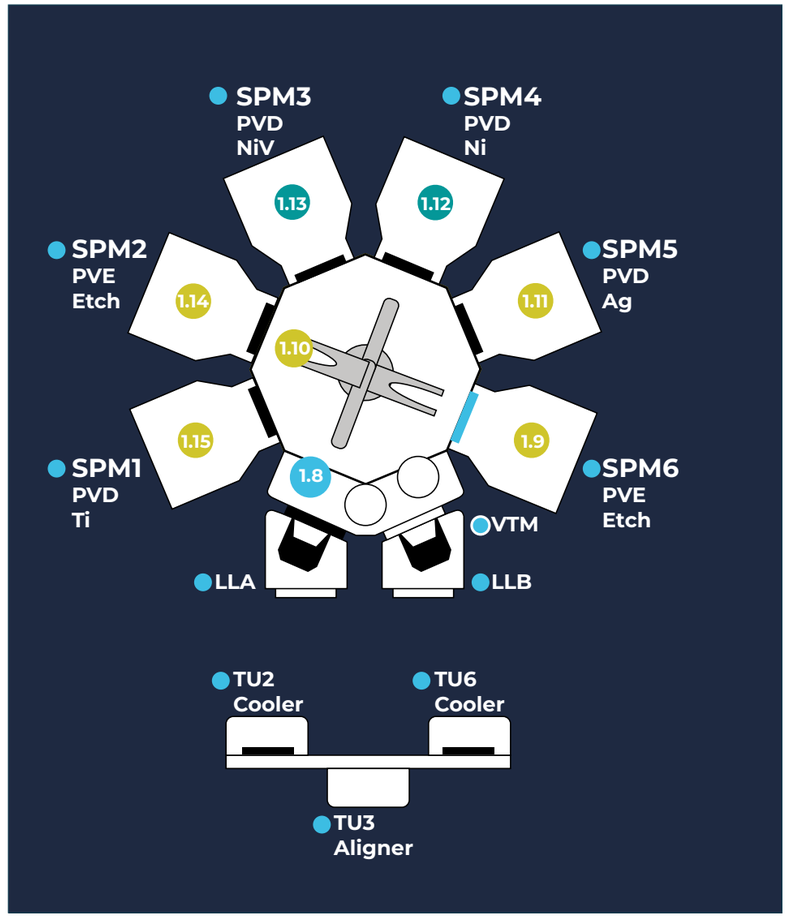
These collaborations, ranging from joint ventures on wafer production to localized device packaging, help transfer process know-how while supporting domestic capacity growth. At the same time, IDMs such as Sanan IC, HHGrace, BYD Semiconductor, and InventChip are scaling 6-inch lines and preparing 8-inch SiC pilot lines in provinces like Hunan and Fujian. The move toward 8-inch wafers is expected to bring cost reduction and volume scalability.

Within this ecosystem, metallization steps are essential. Ti and Ni layers form ohmic contacts and silicides, backside metals provide thermal management, and Ag-based solderable tops enable reliable interconnection. As the SiC industry enters the 8-inch era, advanced PVD tools capable of depositing Ti/NiV(Ni)/Ag stacks with high throughput, uniformity, and flexibility will be vital to support both local manufacturers and international partnerships driving the EV revolution.

1. Full automation with single process modules

Evatec's solution is its CLUSTERLINE® 200 & 300 family equipped with single process modules (SPM). An example of CLUSTERLINE® 200 is shown in Figure 1. Unlike traditional batch systems, the SPM architecture provides complete flexibility in configuring ICP etch, Ti, Ni, NiV, and Ag deposition modules on one platform. This eliminates cross contamination between metals, a critical factor in SiC MOSFET frontside and backside metallization where adhesion layers, ohmic contacts, and solderable tops are integrated in a single flow.

Moreover, the creative TU (Treatment Unit) design enables customers to integrate functions such as degas, cooling, RGA (Residual Gas Analyzer), wafer alignment, and dummy wafer storage in the transfer module without occupying the chamber slot.



Flow steps

- **Step #1 (Aligner)**
  - default
- **Step #2 (Exclusive)**
  - SPM_SPM2
  - SPM2_NtveOxRmvl
- **Step #3 (SPM_SPM1)**
  - SPM1_Ti
- **Step #4 (SPM_SPM3)**
  - SPM3_NIV
  - Step #5 (SPM_SPM5)
  - SPM5_Ag
- **Step #6 (Exclusive)**
  - TU_TU26
  - TIOG AA AGAA

Figure 2:
Left: Intuitive Evatec eXperience Operation GUI, configured a PVD equipment for BSM, STM and Silicide processes.
Right: Process flow design for BSM process.

The different metallization process types are clearly defined within Evatec's CLUSTERLINE® 200/300 platform:

- **BSM (Backside Metallization):** ICP/Ti/Ni(NiV)/Ag stacks designed for solderable and thermally conductive backside contacts
- **STM (Solderable Top Metallization):** ICP/Ti/Ni(NiV)/Ag stacks optimized for robust front-side interconnects
- **Silicide Formation:** Ti or Ni deposition for ohmic contacts, enabling low-resistance interfaces
- **Optional FSM (Frontside Metallization):** ICP/Ti/TiN/AlCu stacks featuring up to AR 5:1 trench fill capabilities

A single CLUSTERLINE® tool (Figure 2) can be configured to handle BSM, STM, Silicide, and FSM modules simultaneously, giving customers maximum flexibility in their device roadmap. This is enabled by a specially designed modular chuck, which satisfies the no-scratch requirement essential for BSM processes on thick and sensitive SiC wafers, while also being robust enough to support STM and Silicide processing. Moreover, the architecture allows for additional ICP etch chambers to be configured, providing in-situ surface cleaning or etch capability before metallization.

Each module offers precise wafer handling, cassette-to-cassette automation, and state of the art recess chuck technology, ensuring wafer safety and process repeatability. For customers, this translates into stable film uniformity across 200 mm substrates, tighter process windows, and straightforward recipe fine tuning for new device generations. Furthermore, single process modules inherently require fewer clean parts compared with batch chambers, which reduces maintenance downtime, lowers consumable costs, and ensures longer mean time between cleans. This balance of flexibility, performance, and reliability sets the Evatec platform apart for power device fabs moving into 8-inch SiC. Process performance data is reported in Figure 3.

Stack	SPM	Rate	Uniformity 1sigma	Stress MPa
Pre Clean	SPM2 + SPM6	400 A/min	6.13%	~-300
Ti	SPM1	40 A/s	1.8%	~50
NiV	SPM3	130 A/s	1.4%	~200
Ag	SPM5	95 A/s	1.99%	~0
Cool	TU2 + TU6			

Figure 3: Real process sampling data for ICP/Ti/NiV/Ag process flow, result in 35.1 wafer/hour on 8-inch SiC applications.

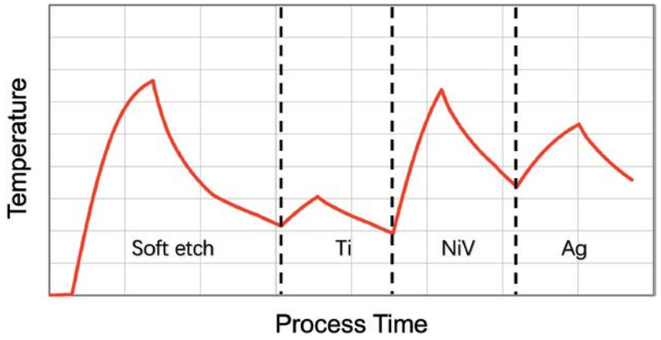


Figure 4: A typical simulation sample that Evatec will provide to estimate the process maximum temperature, throughput according to substrate and layer stack information.

2. Process temperature simulation capability

Another critical advantage is the ability to simulate process temperature conditions before a tool is even installed at the fab (Figure 4). By modeling the substrate type, wafer thickness, and target layer stack, engineers can calculate peak wafer temperatures at specific deposition rates and then correlate these with wafers-per-hour (WPH) throughput.

This unique service enables customers to predictively evaluate their process integration flow, avoiding surprises during ramp-up. For example, in high-aspect-ratio metallization or backside deposition on thick SiC wafers, process thermal budgets are tight. Simulation demonstrates how throughput and deposition rates influence peak wafer temperature, ensuring that neither R_c degradation nor film stress compromises device performance.

Customers gain a detailed understanding of process limitations and opportunities during the evaluation stage, accelerating decision-making and shortening time-to-market.

“Evatec doesn’t just deliver hardware – it delivers actionable process intelligence that de-risks investment and guarantees optimized production from day one.”

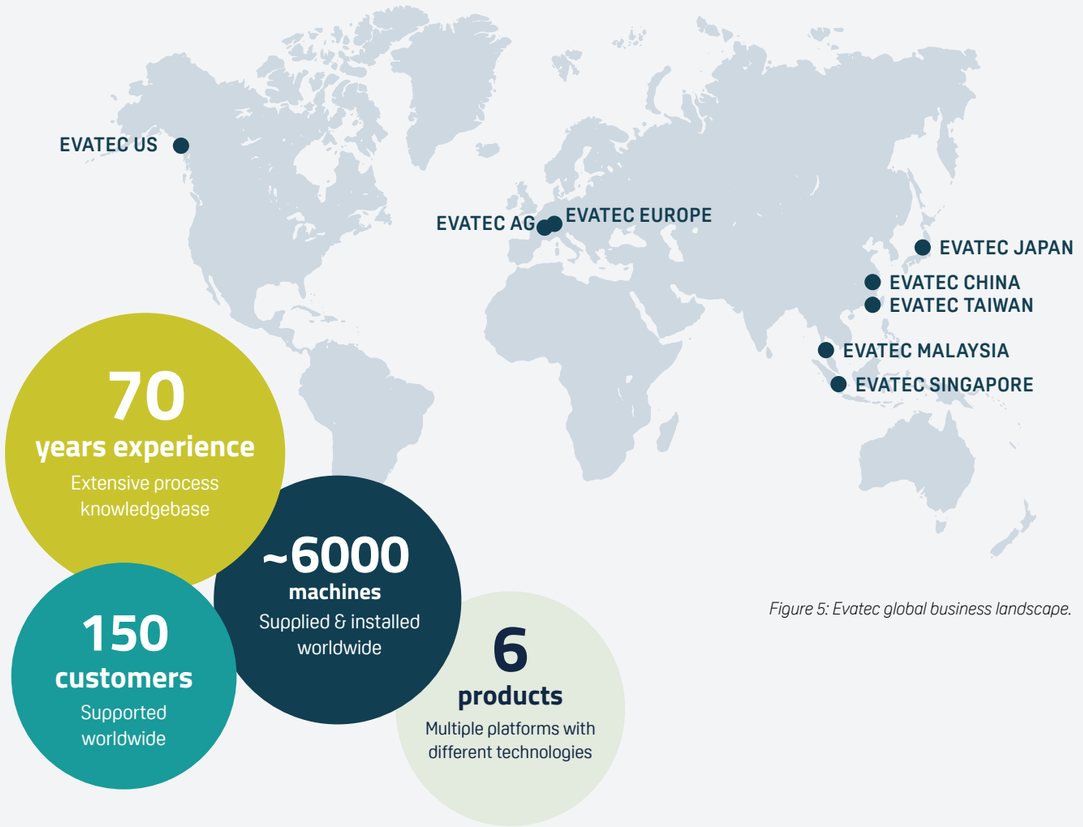


Figure 5: Evatec global business landscape.

3. A strong Customer Service team – from local offices to headquarters

Equally important to technology is the service infrastructure supporting it. As part of its global Sales and Service Oganization (Figure 5), Evatec has invested heavily in its Asia operations since 2017, building a dedicated group of around 100 semiconductor professionals. These engineers and managers are well-educated, with backgrounds spanning process, software, and hardware disciplines.

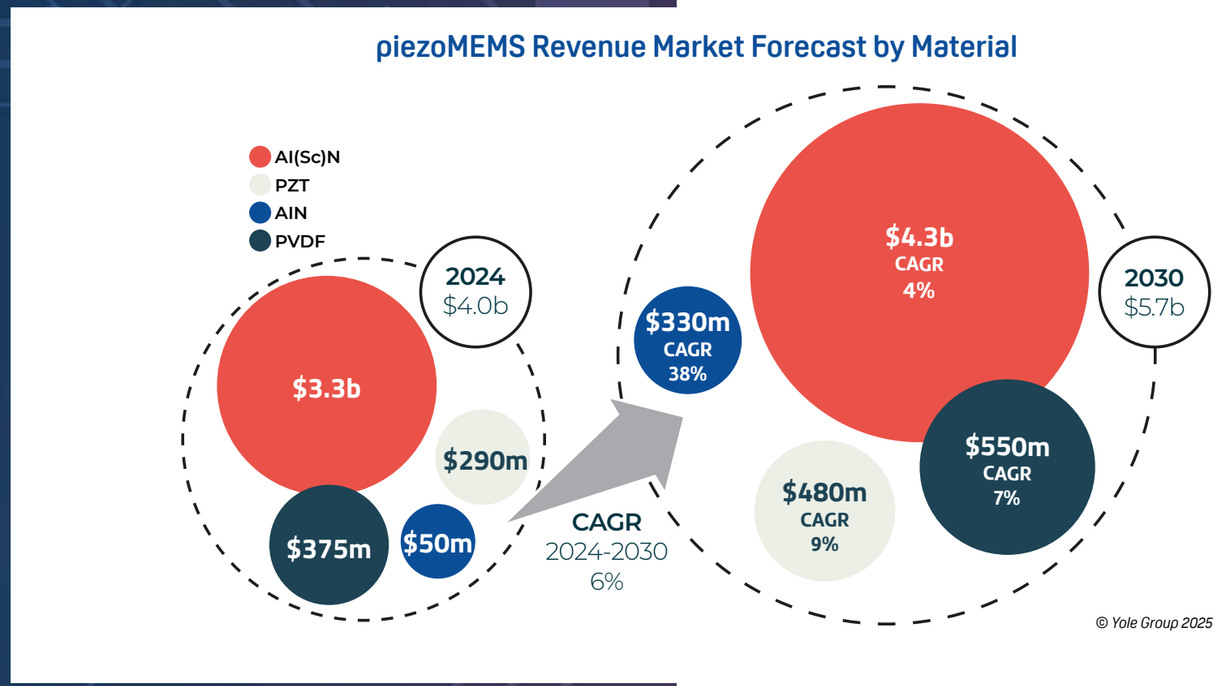
Their mission is to provide fast, professional responses to Asia customers, from OSATs and IDMs to emerging SiC device makers. Service offerings include installation, troubleshooting, performance optimization, and critically design of experiments (DOE). DOEs can be coordinated directly with the headquarters in Switzerland for advanced cases or designed and executed locally to ensure the fastest reaction speed in tackling customer challenges.

This hybrid model gives fabs direct access to Evatec’s global process expertise while maintaining the agility of a local support team. Customers therefore benefit from rapid turnaround during qualification and production ramp, minimizing downtime and ensuring maximum equipment utilization. The presence of spare parts warehouses, technical training, and an Asia Technical Task Force (ATTF) further strengthens Evatec’s ability to deliver world-class service in the region.

Conclusion

The combination of single process module flexibility, predictive temperature simulation, and an experienced local support organization makes Evatec the partner of choice for fabs scaling to 8-inch SiC MOSFET and power device production. As international and domestic players push to secure leadership in EV, renewable energy, and industrial power markets, Evatec’s CLUSTERLINE® platforms provide the process stability, transparency, and service responsiveness required for success. By uniting Swiss engineering precision with Asia service strength, Evatec ensures that customers can confidently meet the demands of next-generation power electronics with the lowest cost of ownership and highest reliability.

COMPOUND & PHOTONICS



The rise of piezoMEMS:

Vibrant opportunities and challenges

After a wide adoption in RF filters, piezoMEMS are powering the next generation of microspeakers, oscillators, optical switches, and microcooling devices.

Piezoelectricity is a physical phenomenon that has been utilized for nearly a century. Thin film deposited materials, such as PZT, AlN (with or without Sc doping), KNN, $LiNbO_3$, and PVDF, are now being widely applied across various industries. Depending on the application, piezoelectric-based components can be used for sensing, actuation, or signal transduction (physical to electrical or vice versa). The piezoMEMS device market was valued at $4 billion in 2024 and is projected to grow to $5.7 billion by 2030, at a 6% $CAGR_{24-30}$.

Today's snapshot is based on the sensing collection of reports offered by Yole Group. This collection includes the annual report, Status of the MEMS Industry 2025, as well as PiezoMEMS Technologies 2025, Microphones, Microspeakers and Audio Processing 2025, Sensors and Actuators for Wearables 2025, Greater China MEMS Industry 2025, PiezoMEMS Comparison 2025.

MEMS devices based on piezoelectric materials are primarily used in applications such as RF filters, inkjet printheads, microphones, voice accelerometers, microspeakers, micromirrors, timing oscillators, ultrasonic fingerprint sensors, and ultrasonic pMUTs (used in imaging, radar, cameras, and Time-of-Flight systems). Among these various devices, significant advancements are expected in MEMS microspeaker technology.

In contrast to the well-established MEMS microphone market, which reached nearly seven billion units in 2024, the MEMS microspeaker market is still in its early stages of adoption, with two million units sold in 2024. MEMS microspeakers compete with well-established legacy technologies such as electrodynamic speakers (ES) and balanced armature (BA) speakers.

With the ability to be integrated in TWS earbuds, Smart Glasses, AR headsets, and Smartwatches, MEMS microspeakers offer several advantages over traditional technologies. These include lower power consumption, high repeatability and uniformity, greater assembly reliability, immunity to dust and water, and the potential for a lower average selling price (ASP) through economies of scale. The MEMS microspeaker market was worth $3.9 million in 2024, representing approximately two million units, and is expected to grow at a 79.8% $CAGR_{24-30}$.

Companies such as xMEMS, USound, and AAC Technologies are leading players in the MEMS microspeaker market, with xMEMS and USound together accounting for 93% of the market. Both companies use piezoelectric PZT thin-film layers in their product designs for actuation purposes. This PZT layer is typically deposited using the physical vapor deposition method (USound – Conamara) or the sol-gel spin-coating method (xMEMS – Montara, Cowell; USound – Achelous). (A detailed analysis of these devices can be found in our comparison report, PiezoMEMS comparison 2025). While xMEMS and USound already have products available on the market, several other companies are actively developing their solutions, aiming for market entry in the coming years, including Bosch Sensortec, Sonic Edge, MyVoX, and Fortémedia.

About the Author

Clyde Midelet, PhD, is Senior Technology & Market Analyst at Yole Group.

Working within the Sensing, Imaging, and Display activity, Clyde contributes daily to technology and market analyses as well as the development of relevant products. He is also involved in custom consulting projects at Yole Group. His expertise spans various areas, including microfluidics, sensing, and MedTech.

After completing his master's in solid-state chemistry at Rennes University in France, Clyde pursued a PhD at the École Normale Supérieure de Rennes in collaboration with the SATIE laboratory in France.

During his research in microfluidics, which resulted in various scientific papers, Clyde developed a system for the electrical manipulation of gold nanoparticles for biosensing in in-vitro diagnostics. Additionally, he worked on an industrial project related to next-generation displays using quantum dot technology.

Characteristics	U SOUND	MEMS		BOSCH	SONIC EDGE
Technology	Piezo actuator with plastic membrane	Piezo membrane	Modulated ultrasound	Electrostatic membrane	Modulated ultrasound
Sensitivity to vibration	Medium	Medium	None	Medium	None
PCB assembly possibility	YES	YES	YES	YES	YES
Bass audio quality	N/A. 2 ways audio system used: 1 MEMS for tweeter + 1 legacy for the woofer	N/A	Possible	N/A	Possible
Mid audio quality	YES	YES	YES	YES	YES
Treble audio quality	20 kHz	40 kHz	40 kHz	20 kHz	40 kHz
HD audio	NO	NO	YES	NO	YES

This table shows that ultrasound modulation technology brings several advantages
©Yole Group 2025

One of the key challenges for MEMS microspeakers is achieving full-range audio performance across the entire frequency spectrum. The most promising approach to address this challenge is modulated ultrasound (a technology being explored by Sonic Edge and, more recently, xMEMS). Another viable solution for achieving high sound quality is a 2-way speaker system, where a MEMS device is used as a tweeter, paired with a legacy woofer. This is the approach adopted by USound.

While piezoelectric materials show strong promise in MEMS microspeakers, this represents just the tip of the iceberg in terms of broader application opportunities. Piezoelectric technologies are also of interest in several other sectors:

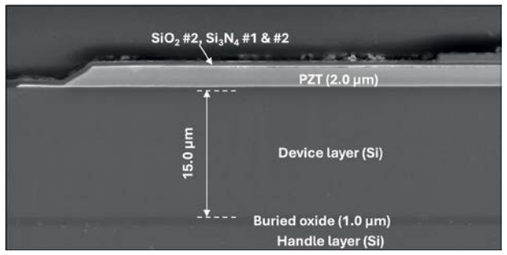
→ **Telecom:**
Future innovations such as 6G networks and Wi-Fi 8 will require new filter technologies, including XBAR (Murata) and XBAW (Akoustis*), both based on piezoelectric effects.

→ **AI & Data Infrastructure:**
- Development of high-precision timing solutions for data centers (e.g., SiTime)
- Deployment of optical switches (e.g. micromirrors) to reduce power consumption and increase bandwidth (e.g., Google, nEye)
- Emerging microcooling solutions to support high-performance computing in data centers and consumer devices (e.g. xMEMS, MyVox).

An entire ecosystem is emerging around piezoMEMS technologies. Foundries are advancing their expertise in piezoelectric thin-film deposition to better address the challenges of this growing market. They are now mastering deposition quality, increasing production capacity to meet market demand, and proactively addressing future challenges such as material restrictions related to lead content by offering alternative, lead-free solutions.

The latest report from Yole Group, "PiezoMEMS Technologies 2025", provides detailed insights into the market and technology trends that are poised to offer promising opportunities for the PiezoMEMS industry. This analysis is part of a collection of reports on sensing topic offered by Yole Group.

Achelous from USOUND



MEMS Membrane Cross-Section – SEM View
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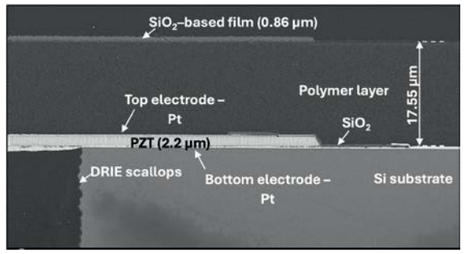
Conomara from USOUND



MEMS Membrane Cross-Section – SEM View
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Related Yole Group's products
- *Status of the MEMS Industry 2025*
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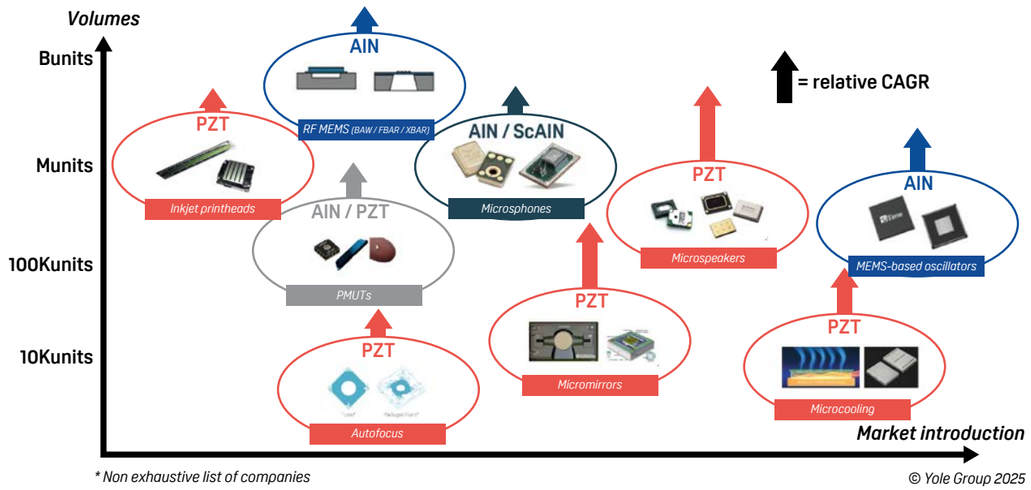
- *Sensors and Actuators for Wearables 2025*
- *Greater China MEMS Industry 2025*
- *PiezoMEMS Comparison 2025*

** Acquired by SpaceX*

Source: www.yolegroup.com

piezoMEMS Popularity

Increase of the use of PZT, AIN and ScAIN materials*



** Non exhaustive list of companies*
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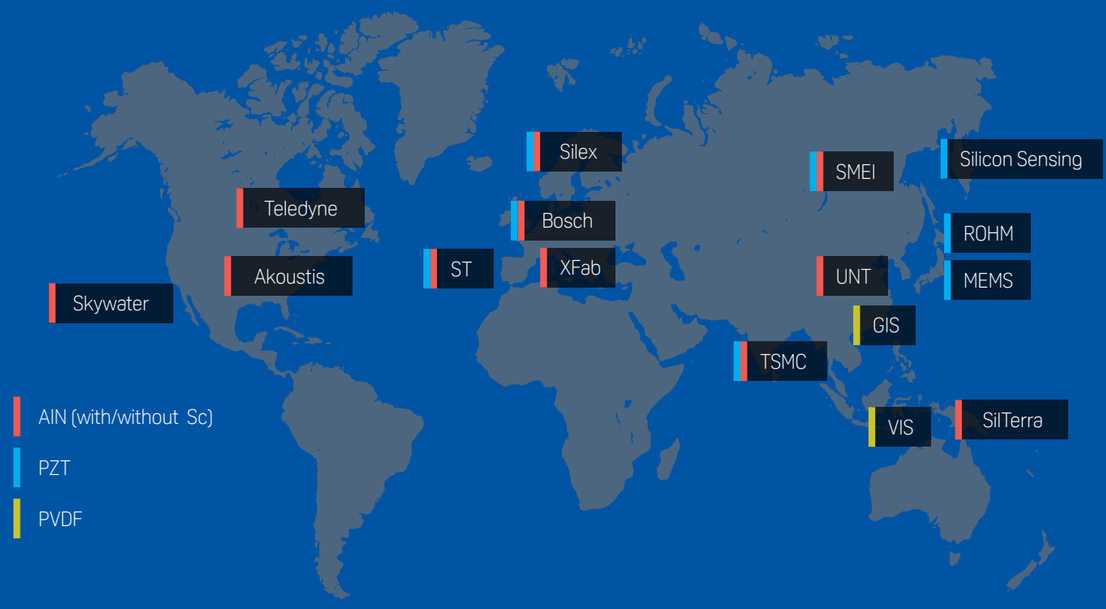
MEMS foundries with thin-film piezoelectric capabilities*



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PZT

a long history and an exciting future

With its inherent advantages over sol-gel processing, PVD deposition of lead zirconium titanate has been a mainstay of the MEMS industry since Evatec delivered its first tools and set up its first industry collaborations over 15 years ago. With the recent growth in demand, including for areas like micro speakers, micro mirrors and air coolers, Evatec Product Marketing Manager, **Dino Faralli**, and Process Engineer, **Volker Roebisch**, explain the manufacturing challenges and the new options available to customers today according to their production throughput.

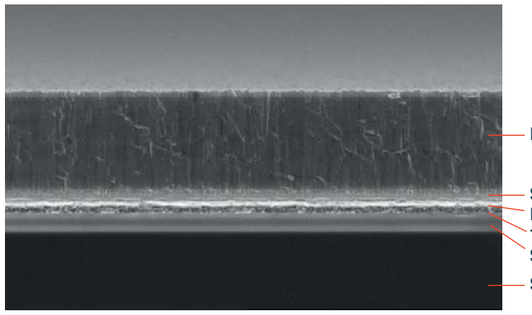


Figure 1: Typical PZT layer stack comprising adhesion layer, diffusion barrier, conductive electrode, and seed layer for film growth in perovskite crystal structure.

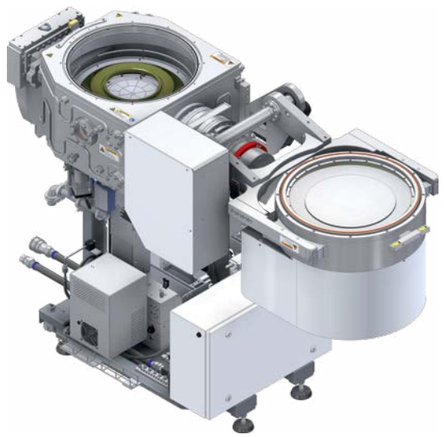


Figure 2: New RF process module for 400 mm targets integrating Very Hot Chuck and substrate bias tuning technology.

Figure 3: Picture of CLUSTERLINE® 200.

It's a complex process

The deposition of the PZT layer is just one part. A sequence of layers is needed to enable the PZT to grow with the correct stoichiometry and the needed crystal structure and orientation.

The stack

Figure 1 shows a typical stack comprising a metal / metal oxide stack for good adhesion and as diffusion barrier, a platinum electrode for electrical contact, and an oriented seedlayer to serve as template for the crystal structure prior to deposition of the PZT, for which deposition process and layer properties must all be first optimized to ensure best end-layer performance.

Process specifications on 200 mm call for high dielectric polarization and large piezoelectric response, but also typically for low wafer stress < ± 250 MPa (to ensure low wafer bow), low leakage current, high fatigue resistance less than 5% at 1e10 cycles, and tanΔ less than 5%.

The Evatec PZT process kit

The Pb $[Zr_xTi_1\text{-}x]\ O_3$ ceramic target composition with a dopant at low concentration is carefully chosen to improve the dielectric properties. RF sources for large targets of 400 mm diameter (Figure 2) are specified for competitive film uniformity. A dedicated magnet pack and new RF shield design are combined with a "Very Hot Chuck" for reliable operation at temperatures beyond 500°C in daily production. A newly integrated matching unit with autotuning allows adjustment of film properties and precise process control.

CLUSTERLINE® 200 – A proven workhorse for PZT production

In its largest configuration, today's CLUSTERLINE® 200 (Figure 3) can be equipped with up to 6 process modules for etch and deposition, plus three additional stations for integration of additional capabilities like degassing and cooling.

However, platform design flexibility now enables customers to choose from a range of options according to their PZT throughput requirements.

High-volume manufacturing

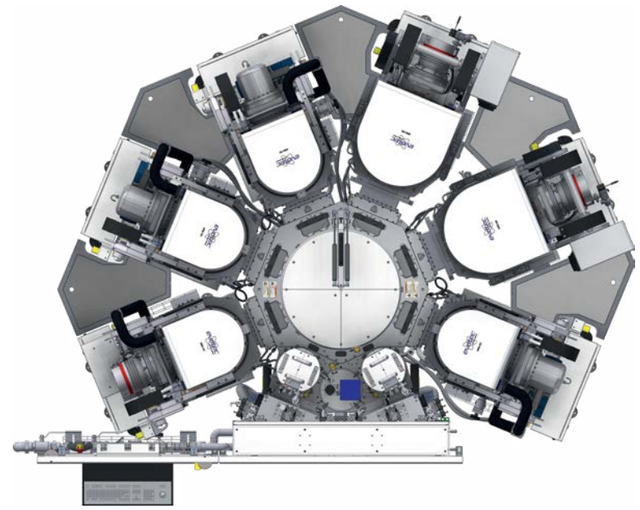
Here, it still makes sense to have dedicated single process modules for each process step, with the option for a second module dedicated to PZT for even higher throughputs (Figure 4).

The enlarged ARQ 320RF process sources used especially for this application deliver the wafer-in-wafer (WiW) uniformities required and a dedicated matching unit allows controlled ion bombardment of the substrate for process tuning.

Development / low volume production

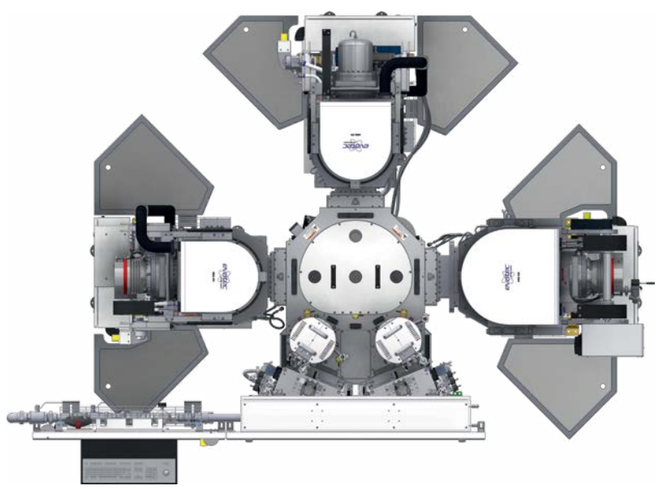
Where demand is lower or budget constraints apply for R&D or low volume production, CLUSTERLINE® 200 can be delivered incorporating Evatec's proven Multi-Source technology for deposition of the metal / metal oxide and seed layers.

- **Option 1:** Using the same 8-sided VTM8 as the high-volume manufacturing platform at its core, the number of process modules could be reduced to 3, leaving room for later expansion.
- **Option 2:** A smaller 5-sided VTM5 platform can also be configured with single and multisources to enable the complete process (Figure 5).



- VTM8 (Aligner, Degas, Cooler)
- 5x SPM: Etch/Ti/Pt/Seed/PZT/PZT*
*optional second SPM PZT for enhanced throughput

Figure 4: Fully equipped CLUSTERLINE® 200 for volume production of electrode, seed and PZT layers. Optionally a second PZT module can be configured for higher throughput.



- VTM5 (Aligner, Degas, Cooler)
- 3x SPM: Etch/MSQ/(Ti, Pt, Seed)/PZT

Figure 5: Budget configuration of a CLUSTERLINE® 200 for R&D and production. 3 SPM including 1 Multi-Source (MSQ) for depositions of electrode, seed and PZT layers.

Take a look at the results

1. Process and piezo-electric performance

Figure 6 illustrates the typical process performance achieved for PZT films. The film stress can be tuned by process parameters with good WiW uniformity, the permittivity is lower than that obtained for sol-gel films, polarization P_{max} is high with low coercive field, breakdown field, and piezoelectric coefficients are aligned to state-of-the-art values but are also a matter of ongoing optimization work. Short-term goals for further process development are also indicated in Figure 6. We are working on them together with partners.

Some of the parameters listed in Figure 6 are reported in more detail in Figure 7. Measurements were done at Silicon Austria Labs in Villach, using a DBLI system from AixACCT, on PZT 1 µm thick, with Pt top electrodes at diameter 1 mm.

2. Crystallinity

Figure 8 confirms the perovskite texture of the prerequisite seed layer with 100 orientation, measured at different radii on 200 mm wafers (Note: result at radius 30 mm is shown).

For PZT, the trace in Figure 9 shows XRD results at different radii on a 200 mm wafer deposited at 550°C and confirms the successful promotion of (100)-textured film growth from seed layer to PZT film.

3. PZT film composition

Figures 10 and 11 show lead and zirconium content as a function of radius on a 200 mm substrate as measured by X-ray Fluorescence (XRF) for a doped target and illustrate how composition can be controlled successfully.

Item	Demonstrated Properties (PZT on Seed layer)
PZT film	200 mm wafer, up to 2 µm, (100) texture
Thickness uniformity 1σ EE6	3.5% (Goal is <3%)
Residual stress	75 MPa (average), Range 50 MPa
Relative permittivity ε_r	800
Breakdown field	500 KV/cm (50 V/µm)
Polarization P_{max}	60 µC/cm²
Remanent polarization $2P_r$	40 µC/cm²
Coercive field	50-60 KV/cm
Leakage	50-60 nA/cm² @ 1V
e31,f	14 C/cm² (Goal is 16C/cm²)
d33,f	100-120 pm/V (Goal is 120 pm/V)
Fatigue	>10^{10} cycles at 5 Hz

Figure 6: Typical values for PZT film properties.

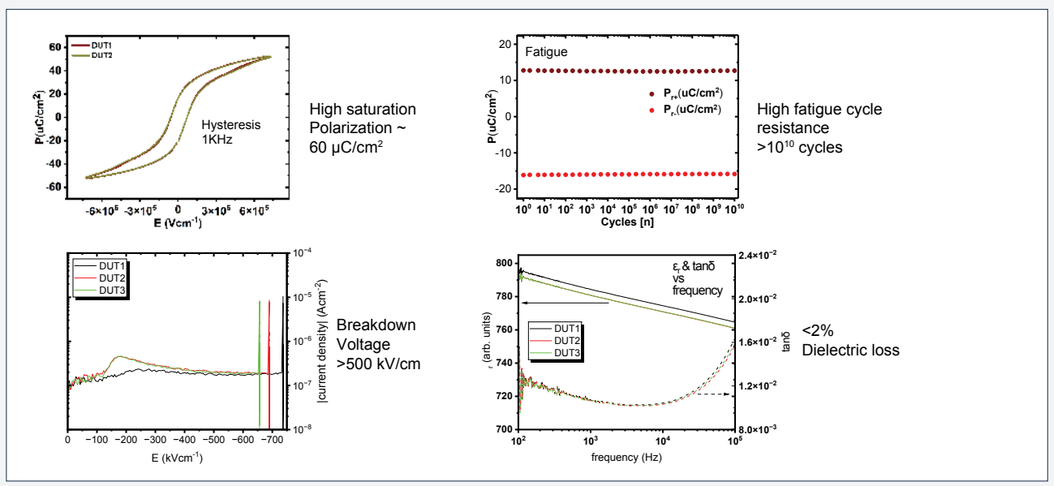


Figure 7: High saturation polarization and breakdown voltage paired with low dielectric losses and very low fatigue best describe the PZT films produced in Evatec's new RF module.

The work continues

As interest grows in improving know-how and processes for PZT, Evatec is continuing to work with partners in optimizing industrial-scale production.

From higher deposition rates to increase wph throughput, to maximizing tool uptimes by reducing target change over times and maximizing shield lives, we are working with our partners in test and qualification. If you would like to learn more about our PZT program, contact your local Evatec sales and service organization today.

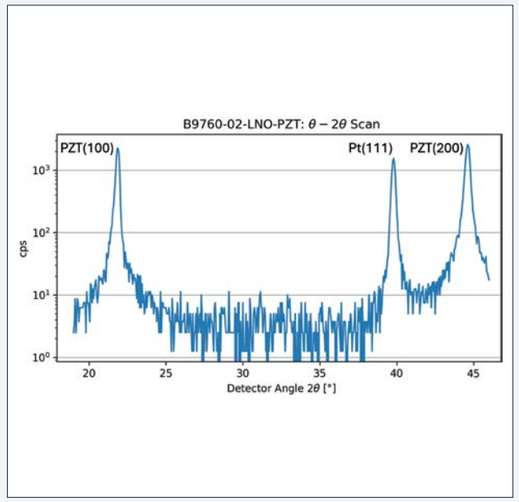


Figure 8: The XRD diffractogram shows a highly oriented perovskite crystal structure in (100)-direction for the deposited PZT on the seed layer.

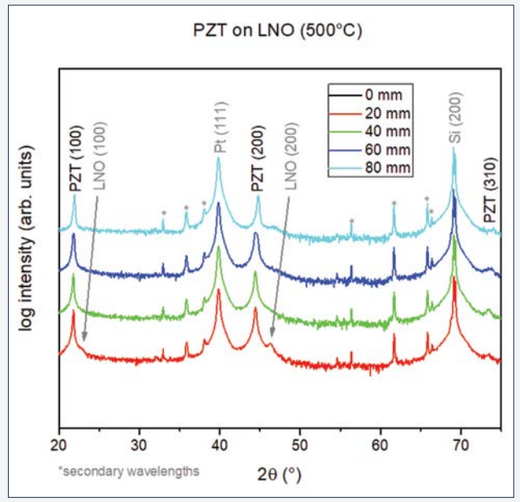


Figure 9: XRD diffractogram indicating highly textured PZT growth out-of-plane in (100)-orientation.

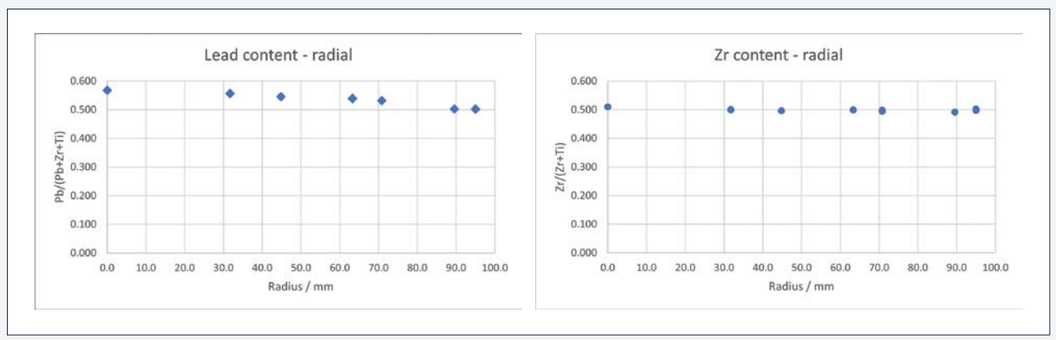


Figure 10 and 11: Radial distribution of Pb and Zr contents in at.-%.

Superconducting thin films for

Quantum Computing

Evatec's Product Marketing Manager, **Dino Faralli**, and Senior Process Engineers, **Dr. Fiodar Kurdzesau** and **Dr. Yaoxuan Feng**, introduce the quantum qubit application areas requiring thin film deposition and how PVD processes such as evaporation or sputtering can contribute to the future of quantum computing.

The role of superconductors

Superconducting thin films are key components in the race to build practical quantum computers based on "quantum bits" (or qubit). Different types of qubit devices are under development. Superconducting, photonic, spin-based, and hybrid as well as superconductors like niobium (Nb), NbTi alloys, tantalum (α-Ta), niobium nitride (NbN), and indium (In) provide the backbone for today's leading approaches. Their ability to carry current without resistance makes them ideal for stable qubits, ultra-low-loss resonators, and reliable chip interconnects. To move beyond laboratory prototypes and toward reproducible wafer-scale production, robust solutions for depositing these materials are essential. Physical Vapor Deposition (PVD) processes such as sputtering, evaporation, and co-sputtering/co-evaporation offer exactly this capability. In the following, we share results achieved on Evatec systems that demonstrate how these technologies can accelerate the path from R&D to scalable quantum hardware.

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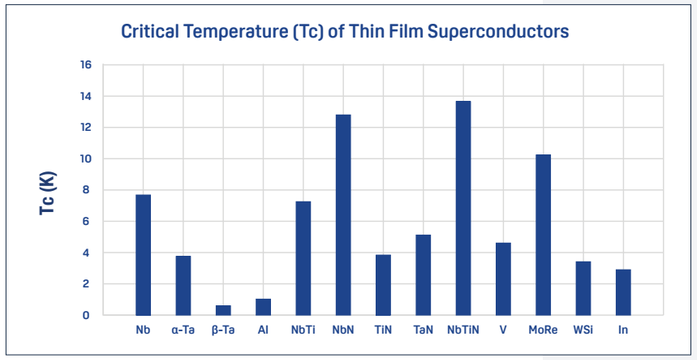


Figure 1: Critical temperature (Tc) of representative thin-film superconductors. Typical Tc values for elemental films (Nb, α-Ta, β-Ta, Al, In, V), alloys/silicides (NbTi, MoRe, WSi), and nitrides (NbN, TiN, TaN, NbTiN) from sputtered, evaporated, or epitaxial thin films, as reported in literature (Liarte, 2020).

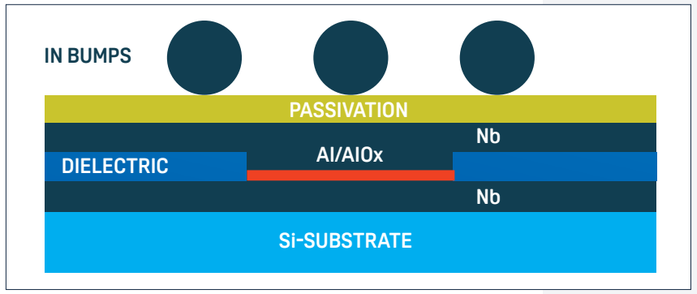


Figure 2: Schematic cross section of a possible implementation for Josephson-Junction qubits.

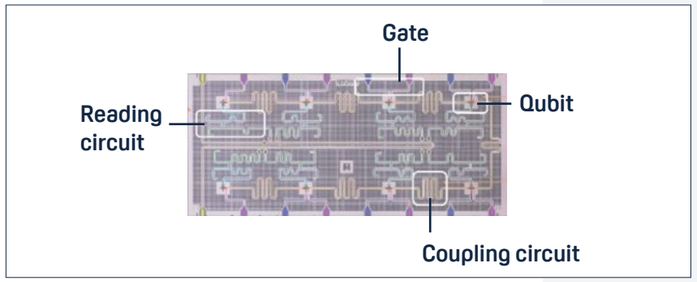


Figure 3: Superconducting qubit processor from https://qudev.phys.ethz.ch/gallery

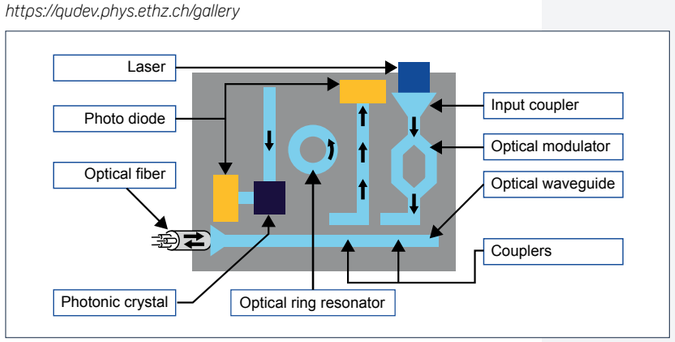


Figure 4: Schematic view of a possible Photonic Integrated Circuit (PIC)

1. Thin films for Quantum Computing

Superconducting materials deposited by PVD can be integrated into all kinds of quantum qubit technologies. Applications can be grouped into three categories: qubit fabrication, circuit interconnects, and hybrid photonic integration.

- **Qubits:** Niobium and Aluminum are widely used in Josephson junction technology, forming the base electrodes and tunnel barriers. Titanium, Titanium Nitride or NbTi alloys with tailored Ti composition provide tunable Tc values suitable for multilayer qubit stacks.
- **Interconnects**: Indium thin films, with their ductility and low-loss properties, are employed as bump bonds and interconnect layers in multi-chip quantum processors. α-Ta can be used as underlayer for superconducting packaging.
- **Hybrid photonic integration:** Scalable circuits where single-photon sources, waveguides, modulators, detectors, and superconducting elements coexist in a compact architecture. They are gaining attention as "photonic qubits" have been proven at relatively "high temperature" (up to 10K) which may reduce the complexity of the cryogenic system. Evatec has solutions for most of these elements, including: superconductors, as listed above, low-loss dielectrics (SiO_2, Si_3N_4), LED lasers and photo-diodes (Si, Ge, HfO_2, Al_2O_3, NbO_2, ITO, GZO, GaN), waveguides (Si_3N_4, AlN) and piezoelectrics (AlScN, $LiNbO_3$, $BaTiO_3$) for optical couplers and modulators. Among the latter, very good results have been achieved from quasi-epitaxial deposition of $BaTiO_3$ (BTO) using a dedicated off-axis sputtering module at 750°C, with resulting high electro-optic coefficient, comparable to one of MBE grown films. The hardware developed for such modules is shown on page 24, LAYERS 9.

2. Sputtering solutions for superconducting thin films

Film properties are shown for Nb and α-Ta sputtered in an Evatec CLUSTERLINE® 200 system on 150mm or 200mm silicon substrates in Figures 6-12. The system was configured as: PVE module for pre-treatment by ICP Ar etch or H_2 soft etch; PVD module with ARQ 151 DC source, Nb 300mm target and water-cooled chuck; PVD module with ARQ 151 DC source, 300mm Ta target and "Very Hot Chuck" for heating up to 750°C; degassing unit at temperature up to 250°C; fast cooling station. The crystallographic structure shown in Figure 6 was characterized by XRD. It strongly affects superconducting behavior. For Nb and α-Ta, body-centered cubic (bcc) structures are preferred. Secondary phases need to be avoided, as these can suppress Tc and increase resistivity. Phase and film purity is thus essential for good and stable Tc. High purity sputtering targets (e.g. Nb 5N and Ta 4N5) were used. The system was equipped with UHV Cryo pumps and the PVD modules were pumped to base pressure P=2*10^{-8} mbar before depositions.

Niobium

Films of thickness 200nm were deposited at nominal room temperature on silicon wafers by DC sputtering, after pre-cleaning by Ar ICP soft-etch. Analysis at XRD shows a polycrystalline film in bcc phase, with (100) peak centered around the expected value ~38.5°, uniform along the wafer diameter (Figure 6).

The deposition rate was set to ~ 2 nm/s at 2 kW DC power. The specific film resistivity at room temperature is ρ ~ 19 μΩ*cm, with measured R_s uniformity within-wafer and wafer-to-wafer less than 1 % (49pts, std dev) on 150mm substrates and 5mm edge exclusion (Figure 7). The superconductive critical temperature (Tc) was evaluated by external partners at values around 9K, in line with state-of-the-art values from literature.

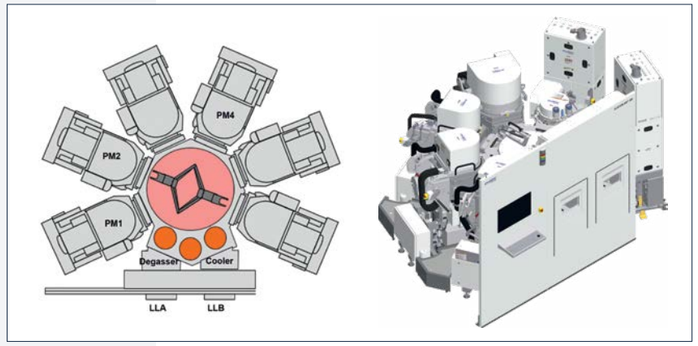


Figure 5: CLUSTERLINE® 200 system configuration for the deposition of Nb and α-Ta superconductors.

- **Degasser**
- **PM2, Etch module**
  Ar ICP etch or H_2 etch
- **PM1, PVD module (Water-cooled chuck)**
  Target: Nb (5N)
  Cathode: ARQ151 DC
- **PM4, PVD module (VHC)**
  Target: Ta (4N5)
  Cathode: ARQ151 DC
- **Cooler**

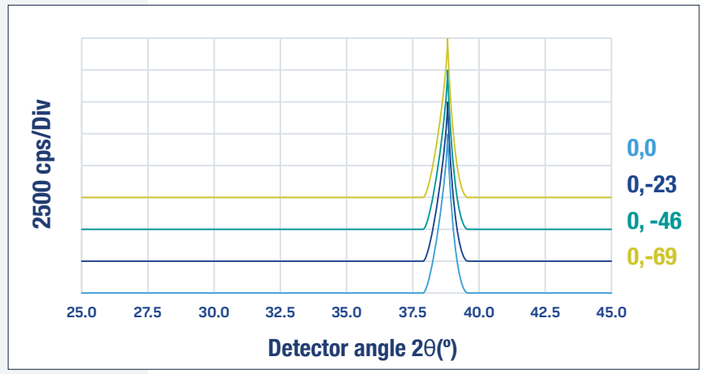


Figure 6: XRD analysis of Nb 200nm film, in 4 positions along substrate radius, position 0 (center), 23mm, 46mm and 69mm. Peak is centered around 38.5° with good uniformity.

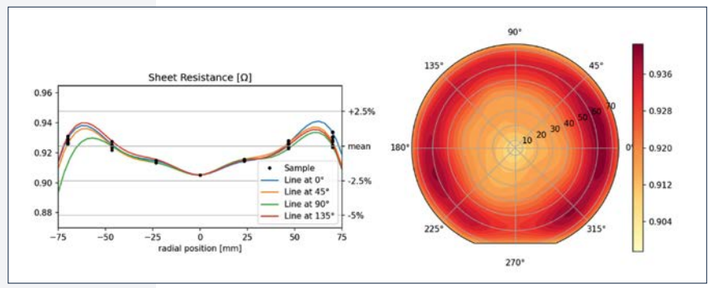


Figure 7: R_s map and uniformity of Nb 200nm deposited on 150mm silicon substrate.

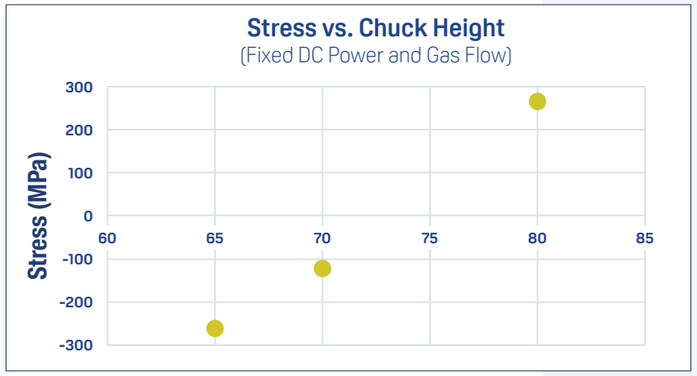


Figure 8: Nb film stress as a function of the wafer-to-target distance (variable chuck height).

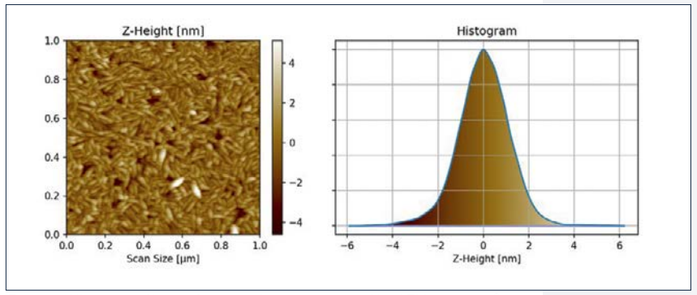


Figure 9: Nb 200nm film surface roughness measured by AFM in 1x1 mm² area.

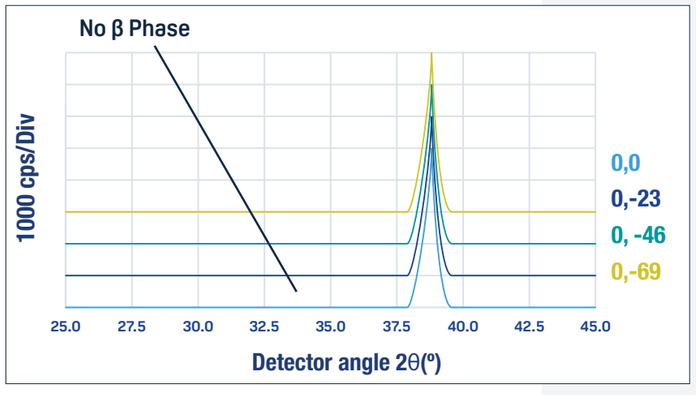


Figure 10: XRD analysis of Ta 200nm film deposited in pure α-phase @600°C over buffer layer: 4 positions on substrate radius, position 0 (center), 23mm, 46mm and 69mm. Peak is centered around 38.5° with good uniformity.

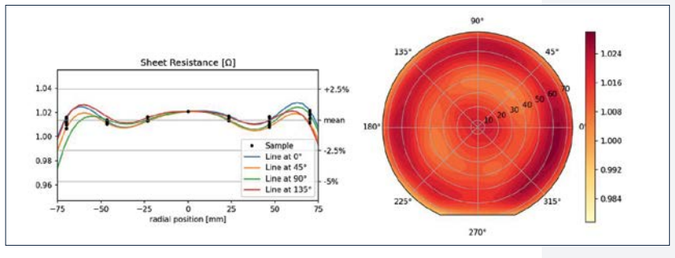


Figure 11: R_s map and uniformity of α-Ta 200nm deposited @600°C over buffer layer on 150mm silicon substrate.

Mechanical stress is a key parameter for device integration. Residual film stress at room temperature is usually preferred to be moderately compressive, to keep the stress low at ultra-low operating temperatures, with improvement of the film stability and Tc. Film stress could be tuned over a wide range from tensile to compressive, by tuning the sputtering parameters, like power density, gas flow and chuck height (Figure 8).

Low surface roughness is another key parameter when integrating stack of films at the extremely uniform conditions required by quantum computing e.g. in the formation of barriers for Josephson Junctions. AFM measurements on scan area 1x1 µm area showed a smooth surface with very good Ra ~0.89 nm and Rq ~ 1.1 nm (Figure 9).

α–Tantalum

For superconducting Tantalum, it is important to deposit it in so-called α-phase, with body-centered cubic (bcc) structure. This is more stable, less resistive and with higher Tc compared to tetragonal β-phase. Deposition at high temperature >500°C is usually enough to get pure α-phase. Films of thickness 200nm were deposited at 550°C and 600°C (using the Evatec "Very Hot Chuck") on silicon wafers by DC sputtering, after pre-cleaning by Ar ICP soft-etch. Analysis by XRD showed a polycrystalline film in bcc α-phase, with (100) peak centered around the expected value 38.5°C, without β-phase peaks. Best results were obtained by deposition on a buffer layer, to avoid interdiffusion of Ta with the silicon substrate at the high deposition temperature (Figure 10). Choosing the appropriate buffer/seed layer leads to pure α-phase even at low deposition temperature.

The deposition rate was set ~ 2.5 nm/s at 2 kW DC power. The specific film resistivity at room temperature was ρ ~ 16 µΩ*cm, with measured R_s uniformity within-wafer and wafer-to-wafer less than 1 % (49pts, std dev) over buffer layer on 150mm substrates and 5mm edge exclusion (Figure 11). The film stress was compressive, with a typical value around -700 MPa (tunable by adjusting sputtering power and gas flow).

The film surface roughness after deposition at 600°C over buffer layer, measured by AFM on scan area 1x1 µm area, showed a smooth surface with very good Ra ~0.81 nm and Rq ~ 1 nm (Figure 12).

3. Co-evaporation of superconducting alloys

50 and 100 nm thick NbTi layers with Ti content between 0 and 50 wt.% were deposited within a BAV 1401 evaporation set-up using two different configurations (2xE-Guns and E-Gun+Thermal boat). The wafers were placed on the spherical calotte with 1050 and 700mm radiuses, where two independently driven E-Gun evaporation sources (Figure 13a) or the combination of E-Gun and Thermal Boat (Figure 13c) were installed (one in the geometrical centre of the calotte (in-axis) for Nb and the second, with 220 mm side displacement (off-axis) for Ti), respectively (see Figure 13b). This geometry corresponds to quasi-"lift-off" conditions and allows reaching >80° material incidence angles when keeping the substrates at room temperature conditions. The films were directly grown on Si and Si/SiO_2 4-inch wafers at 0.5-2.0·10⁻⁶ mBar base pressure using neither adhesion nor capping layers.

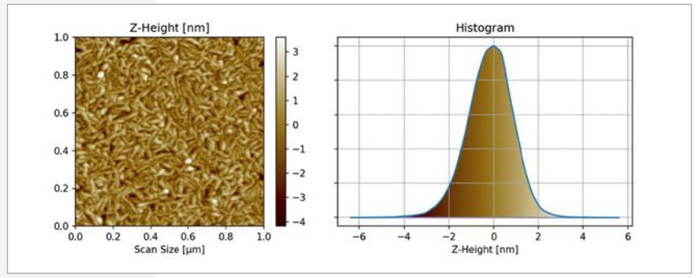
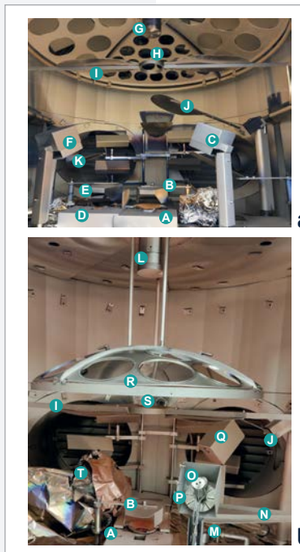
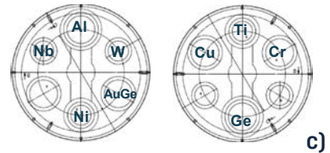


Figure 12: α-Ta 200nm film surface roughness measured by AFM in 1x1 µm² area.



A ESQ 213 central E-gun source (Nb)
B Shutter for central ESQ source
C QSK 300 unit for central ESQ (Nb)
D ESQ 213 side E-gun source (Ti)
E Shutter for side ESQ source
F QSK 300 quartz unit for side ESQ (Ti)
G QSK 1222 quartz unit (monitor)
H Position of sampling wafer(s)
I Fixed 2-fold shaper
J Movable Pivot shaper
K Fixed side shaper (Ti)
L QSK 1221 quartz unit (Nb)
M Thermal boat (Ti)
N Shutter for thermal boat
O QSK 300 quartz unit (Ti)
P Chopper for QSK 300
Q QSK 631 quartz unit (monitor)
R 4x segments calotte R=0.7m
S Thermocouple
T KDC 100 source (covered)



1st E-Gun:
(in-axis for both configurations)

2nd E-Gun:
(configuration 1)

Thermal boat (protected tungsten) filled with Ti (configuration 1)

Figure 13: BAK system for depositing NbTi superconductor: double E-Guns configuration with 1050 mm sample to source distance (a); material arrangement for the co-evaporation tests (b) and E-Gun+Thermal boat configuration with 700 mm sample to source distance (c).

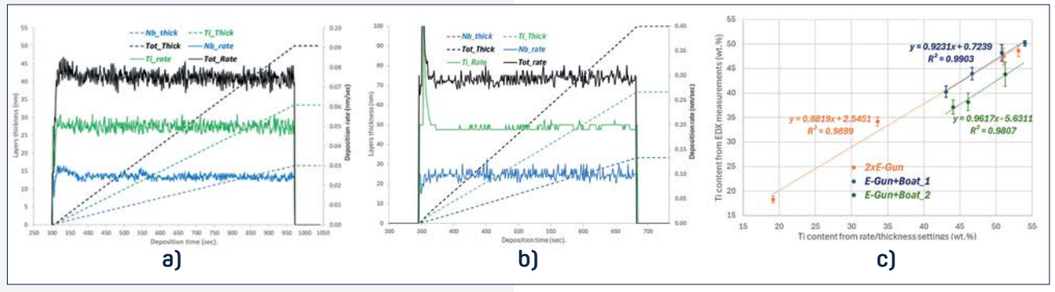


Figure 14: Adjusting of rate and thickness of co-evaporated layers with monitoring quartz crystals in double E-Guns (a) and E-Gun+Thermal Boat (b) configurations, which allows to create the corresponding process calibration curves (c).

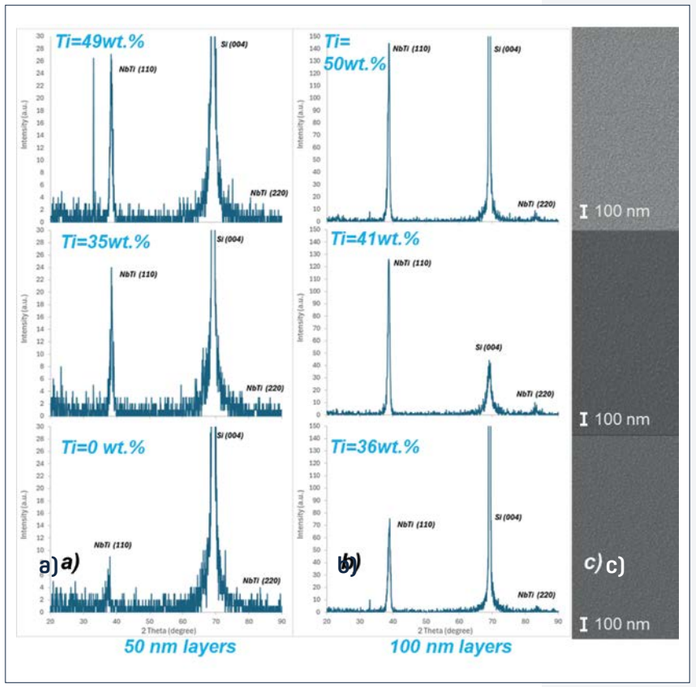
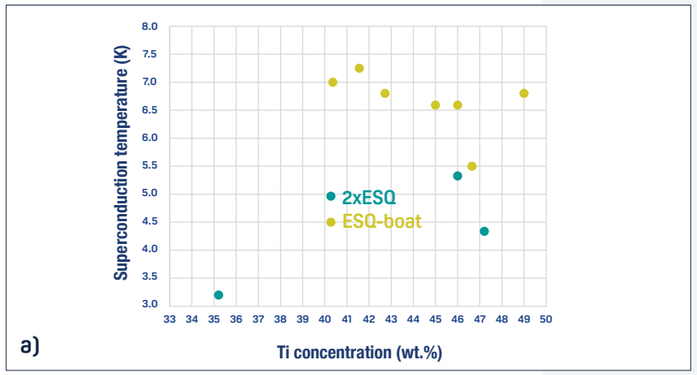


Figure 15: XRD (a, b) and SEM (c) data for NbTi layers from 2xE-gun (a) and E-Gun+Boat (b) processes with 50 and 100 nm thicknesses.



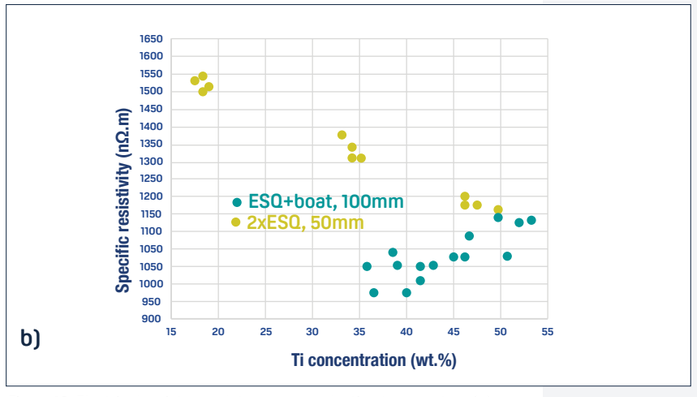


Figure 16: Electrical resistance data: superconducting temperature (a) and specific resistivity (b) as a function of Ti content in co-evaporated NbTi films.

Both co-evaporation techniques used enabled excellent control over the chemical composition of deposited layers. Ti content could be varied in a wide range with good precision by adjusting the deposition rates / thicknesses of co-evaporated Nb and Ti materials (see Figures 14a and 14b) for double E-Guns and E-Gun+Thermal Boat configurations, respectively). The final film composition was verified by EDX measurements, enabling creation and efficient use of corresponding calibration curves for both 2xE-Guns and EGun+Boat configurations (Figure 14c). SEM and XRD analyses confirmed that optimized films exhibit dense structures with increased intensity of NbTi (110) crystalline phase, which also depends on their thicknesses (Figure 15).

The NbTi alloys produced displayed superconducting temperature (Tc) tunability: films having 40–45 wt.% Ti achieved the best performance with Tc ≈ 7.5K. Outside this window, Tc decreased due to the structural disorder or secondary phases (Figure 16a), which also correlates with the layers' specific resistivity values (Figure 16b).

As the long-term stability of superconducting films is critical, corresponding aging tests were also performed. NbTi films with 40–45 wt.% Ti stored under ambient conditions, which simulated two years of device operation, maintained their Tc at a high-level demonstrating robustness against oxidation and contamination (see Figure 17).

Through these results we see that double E-Guns and E-Gun+Boat co-evaporation techniques allow large-scale fabrication of stable superconducting NbTi layers with a variable transition temperature (up to 7.5K). Both processes showed good control and could be used for producing nano- and microscale structures remaining stable in long-term operation at atmospheric conditions. Future process optimization is expected to further improve superconducting temperatures toward the 9K level.

The layers' nitrification by ion-assisted deposition (IAD) in N_2 plasma for their conversion into NbTiN form should also be considered, which could enhance Tc above the 13K level [9].

4. Future Perspectives

The deposition of superconducting thin films, at critical temperature (Tc) up to 15K, is today available by several manufacturing-ready techniques, including PVD sputtering and evaporation.

Similar hardware as used in standard semiconductor processes can be used to fabricate Qubit devices with both Josephson-Junctions or hybrid Photonics approaches, and deposition technology is ready for volume manufacturing.

Research and development into next generation of superconducting alloys (like NbTiN and MoRe) can also take advantage of the Evatec MSQ (Multi-Source-Quattro, Figure 18) co-sputtering module, which enables DC/DC+ and RF/DC depositions from up to four different 100mm sputtering targets at the same time, in Argon or reactive process gas N_2 or O_2, at temperature up to 500°C. Development of a new rotating chuck for deposition up to 750°C (e.g. for α-Ta) is ongoing with the expected first prototype in 2026.

Future device productuion needs may benefit from integration of PVD with ALD and CVD thin film capability in the same deposition system. Extension of the deposition technology to 300mm substrates is also on the road map.

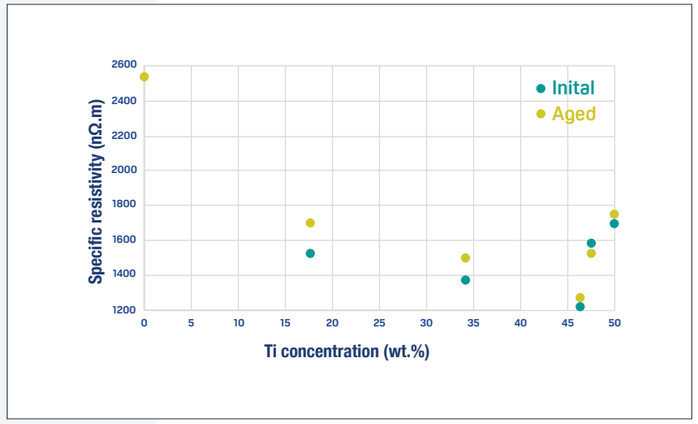


Figure 17: Aging study showing stable specific resistivity of NbTi films after "two years operation" accelerated tests, which correlates with high Tc values (see Figure 16a).

Figure 18: Drawing of the MSQ Multi-Source-Quattro with 3x sources DC/DC+ and 1x source RF/DC for co-sputtering and reactive sputtering of superconductive alloys.

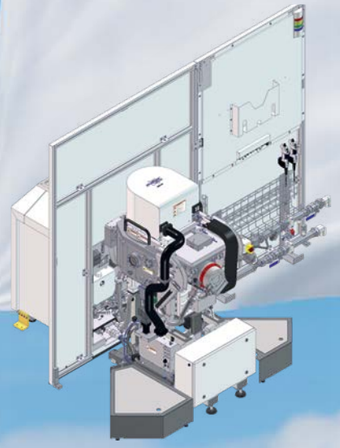
References:
[1] Liarte, Supercond. Sci. Technol. 33, 2020. [2] Heinsoo, Phys. Rev. Applied 10, 2018. [3] Kurdzesau, Gabureac, Kratzer, Heinz, 'NbTi Co-evaporation', Poster E-MRS Spring Meeting, 2025. [4] Barends, 'Coherent Josephson qubit,' Nature, 2013. [5] Krantz, 'A quantum engineer's guide to superconducting qubits,' Applied Physics Reviews, 2019. [6] Devoret, Schoelkopf, 'Superconducting circuits for quantum information: an outlook,' Science, 2013. [7] Kjaergaard, 'Superconducting Qubits: Current State of Play,' Annual Review of Condensed Matter Physics, 2020. [8] Oliver, 'Materials challenges in superconducting qubits,' Journal of Materials Research, 2021. [9] Rezinovsky , Hofer, Sirena, Haberkorn, 'Flexible NbTiN thin films for superconducting electronics,' Physica C: Superconductivity and its Applications, Vol. 607, 2023, 1354241.

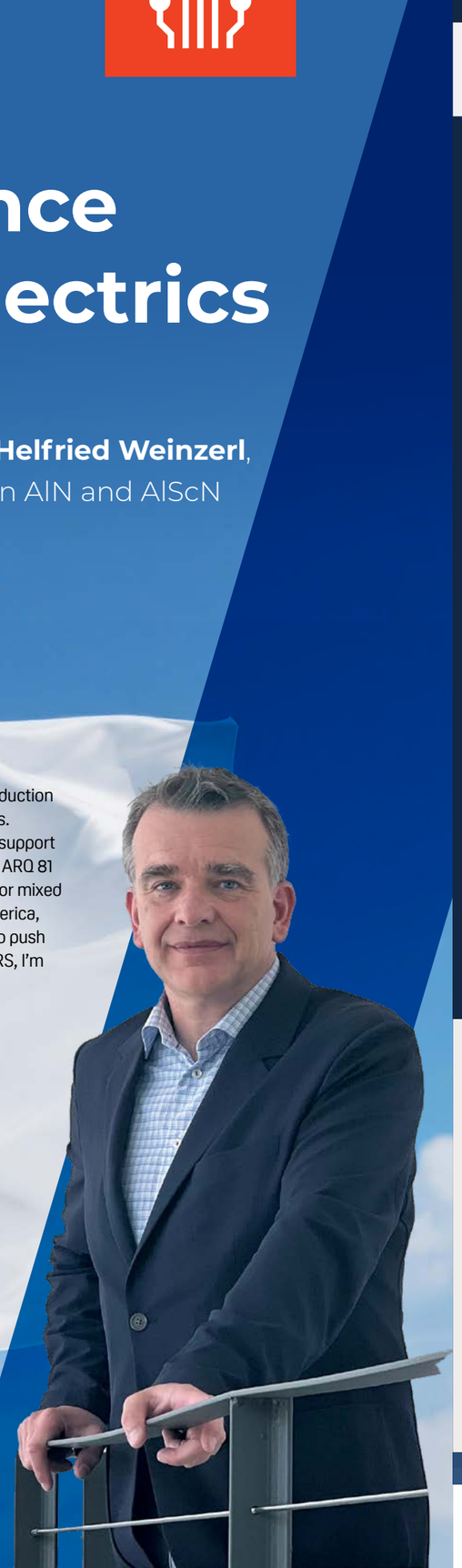
Flying the **high performance ferro- & piezoelectrics** flag in the USA

Evatec North America's Managing Director, **Helfried Weinzerl**, shines a light on some of the leading work on AlN and AlScN being done at universities in North America.

CLUSTERLINE® & MSQ 200 – the perfect tools for development

In its high-volume production configuration, CLUSTERLINE® 200 is already well established in North America and around the world when it comes to mass production of AlN or AlScN for MEMS and Wireless applications on 6-inch and 8-inch wafers. However, it's also available in configurations with process module set ups that support the R&D community. Evatec's MSQ Multi-Source with flexibility to install up to 4 ARQ 81 100mm sputter sources in one MSQ for single target or co-sputtering in DC, RF or mixed modes, is turning out to be an invaluable aid in development work. In North America, we are honored to work with a vibrant community of research groups looking to push the boundaries of ferro- and piezoelectric performance. In this edition of LAYERS, I'm excited to showcase some of the work they are doing.





Penn
University of Pennsylvania

University of Pennsylvania

We chose an Evatec MSQ as the cornerstone purchase in founding our research lab at the University of Pennsylvania. The decision was based on the excellent film quality for Aluminum Scandium Nitride (AlScN) reported by Evatec at the PiezoMEMS workshop and the MSQ's flexibility for rapidly exploring multiple Scandium compositions.

Our research has focused on high frequency AlScN bulk (BAW) and surface acoustic wave (SAW) resonators, filters, and delay lines. One particularly exciting development exploits the ferroelectricity of AlScN to overcome the traditional frequency scaling limits of BAW resonators, where the device layers become too thin. Using periodically poled piezoelectric films (P3F), we achieve frequency scaling while maintaining a nearly constant piezoelectric layer thickness. An example of this concept is shown in Figure 1 below, where for the same 692 nm piezo thickness, the device realized using a P3F material resonates at ~17 GHz, compared to ~4 GHz for the resonator realized in a unipolar film. This approach improves both the small and large signal performance as the operating frequency is increased.

Another major research thrust of our lab has focused on ferroelectric AlScN for non-volatile memory, where we have deposited and characterized ferroelectric films as thin as 5 nm in our MSQ. Even the initial layers of these materials are highly c-axis oriented. The measured breakdown fields exceed 10 MV/cm, demonstrating the high quality and low defect densities possible when sputtering AlScN films in the MSQ. Evatec has been amazing to work with, actively collaborating with Penn on materials research and supporting upgrades to our tool so we can explore new research directions we didn't envision when the MSQ was first purchased.

Troy Olsson is a Professor in the Department of Electrical and Systems Engineering at the University of Pennsylvania. He received his Ph.D. degree in Electrical Engineering from the University of Michigan. He was awarded an R&D100 award for work on Microresonator Filters and Frequency References, the 2017 DARPA program manager of the year, the NSF CAREER award, and the 2022 Bell Labs Prize for his work on Memory Enhanced Computing with III-Nitride Ferrodiodes.

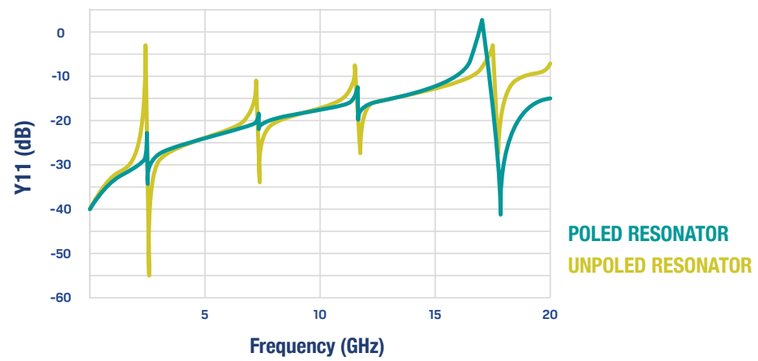


Figure 1: Measured admittance of resonators constructed from unipolar and P3F AlScN of the same thickness. The device realized in the unipolar film exhibits typical BAW operation preferentially resonating in the 1st thickness extensional mode (TE1). The device realized in the P3F film, by contrast, exhibits a strong resonance in the 4th thickness extensional mode (TE4) just above 17 GHz.

Texas A&M University

At Texas A&M University, the Koohi Research Group develops technologies for next-generation (nextG) wireless communication and sensing by advancing acoustic, electromagnetic, and multifunctional microsystems. Our research spans from materials to systems, and from KHz to THz, bridging fundamental material science with device physics and circuit engineering.

We investigate new material compositions, particularly within III-nitrides and complex oxides, to enable acoustic wave integrated circuits (AWICs), reconfigurable RF frontends, and multiphysical microsystems that address the performance and scaling demands of nextG communications and sensing technologies.

The Multi-Source Sputter system provides the foundation for this effort by enabling controlled growth of advanced nitride films and multilayer structures. Its co-sputtering capability allows us to systematically vary composition and stress, tailoring piezoelectric and acoustic properties to meet device requirements. Uniformity and reproducibility across substrates are critical as we transition from exploratory studies of material behavior to the fabrication of high-performance device prototypes.

Our ongoing projects include the development of high-frequency resonators, filters, and integrated modules that operate across sub-6 GHz, millimeter-wave, and emerging sub-THz bands. By coupling material innovation with careful device design, we aim to reduce insertion loss, improve reconfigurability, and achieve compact, energy-efficient architectures suitable for nextG communication systems. Beyond supporting individual projects, the system also strengthens collaborative research across disciplines at Texas A&M. It enables a device, material co-design framework. This integrated approach accelerates the translation of new compositions into practical RF and MEMS technologies, ensuring that materials advances directly inform system-level performance. Such co-design is central to our vision for advancing the next generation of wireless infrastructure.

Prof. Milad Koohi earned his Ph.D. in Electrical Engineering from the University of Michigan in 2020. He led R&D at Qorvo Inc., integrating ferroelectric nitrides into acoustic wave devices for microwave and mm-wave applications. In 2025, he joined Texas A&M University. His research explores multiphysical interactions in emerging materials for advanced devices, microsystems, and integrated circuits. He has received awards including the Qorvo Best New Technology Award and IEEE MTT-S Fellowship, and authored over 40 publications and patents.

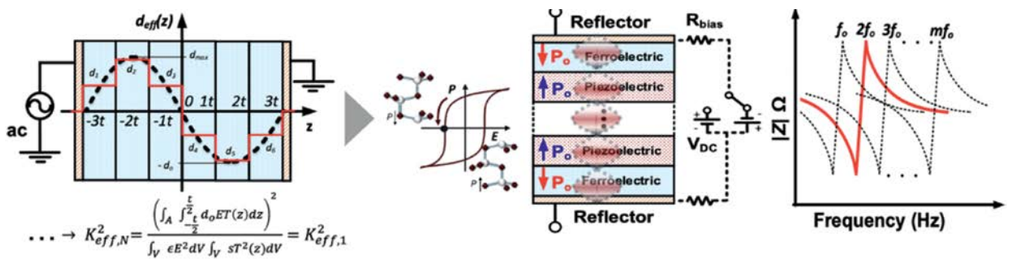


Figure 1: Inhomogeneous piezoelectric media based on multilayer ferroelectric heterostructures enable excitation of harmonic resonance modes with electromechanical coupling comparable to that of the fundamental mode [1], [2], forming the foundation of next-generation mmWave acoustics. This behavior can be realized using ferroelectric III-N materials.

References: [1] M. Z. Koohi and A. Mortazawi, "Negative Piezoelectric-Based Electric-Field-Actuated Mode-Switchable Multilayer Ferroelectric FBARs for Selective Control of Harmonic Resonances Without Degrading K2," IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, vol. 67, no. 9, pp. 1922–1930, Sept. 2020. [2] A. Mortazawi and M. Koohi, "Bulk acoustic wave resonators employing materials with piezoelectric and negative piezoelectric coefficients," U.S. Patent US12206388B2, 2025.

University of Texas

In Prof. Xiuling Li's group at the University of Texas at Austin, AlN and AlScN thin films deposited with Evatec's CLUSTERLINE® 200 are used to create strain-induced self-rolled-up membrane (S-RuM) devices.

The S-RuM platform consists of a strained bilayer deposited on a sacrificial layer that, when etched, releases the strained bilayer and allows it to roll up into a tube, enabling the formation of complex 3D multi-turn architectures with only 2D processing techniques. Sputtered AlN and AlScN can achieve extremely high stresses of >1 GPa and, when used as the S-RuM strained bilayer, allow the shrinking of device footprints while avoiding the pinhole issues associated with PECVD SiNx, a commonly used alternative.[1], [2] By patterning different materials atop the AlN and/or AlScN before rolling, we've demonstrated ultra-small (~0.15 mm^2) inductors with ~1 µH-mm^{-2} and Q/area >100 mm^{-2}.[3] AlScN is also known for its good piezoelectric properties – by integrating piezoelectric AlScN, we've achieved piezoelectrically-actuated tunable S-RuM capacitors with footprints of 0.18 mm^2 and large capacitance tuning ratios for RFICs (see Figure 1). [4] S-RuM devices can further target a wide range of applications including MEMS, passive electronics, biofluidics, and photonics, due to their easily modifiable design with little increase in footprint or process complexity.

By depositing films in the test lab in Switzerland and modifying recipes based on our results, Evatec has enabled us to further push the S-RuM technology into the AlN/AlScN material space, with performance comparable to or better than previous SiNx-based devices. Our new CLUSTERLINE® 200 Multi-Source tool at the Microelectronics Research Center (mrc.utexas.edu) was recently installed, and we're looking forward to trying out the tool for ourselves!

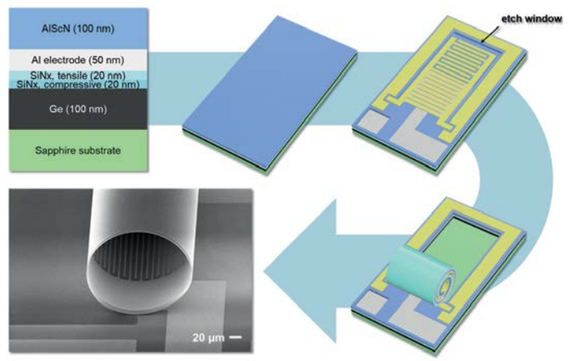


Figure 1: Process flow of self-rolled-up membrane (S-RuM) device based on AlScN thin films.

Kristen Nguyen is a PhD candidate in Prof. Xiuling Li's group at UT Austin. Her work focuses on the piezoelectric and ferroelectric tuning of strain-induced self-rolled-up membranes for high-frequency passives, with several publications on S-RuM passives and piezoelectrically-tunable capacitors and a provisional patent on S-RuM piezoelectrically-tunable passives.

References:
[1] A. Khandelwal et al., "Self-Rolled-Up Aluminum Nitride-Based 3D Architectures Enabled by Record-High Differential Stress," ACS Appl. Mater. Interfaces, vol. 14, no. 25, pp. 29014–29024, June 2022, doi: 10.1021/acsami.2c06637. [2] Z. Yang et al., "S-RuM Technology for Extreme Miniaturization and Integration of Passive Electronics and Microfluidics," in 2024 IEEE 37th International Conference on Micro Electro Mechanical Systems (MEMS), Austin, TX, USA: IEEE, Jan. 2024, pp. 202–205. doi: 10.1109/MEMS58180.2024.10439466. [3] Z. Yang et al., "Unleashing the Performance of Self-Rolled-Up 3D Inductors via Deterministic Electroplating on Cylindrical Surfaces," Adv. Mater. Technol., vol. n/a, no. n/a, p. 2400092, doi: 10.1002/admt.202400092. [4] K. Nguyen, Z. Yang, A. Wang, S. A. Wicker, and X. Li, "Tunable Ultra-Small Monolithically-Rolled-up Capacitors by Piezoelectric Actuation," in 2024 IEEE 37th International Conference on Micro Electro Mechanical Systems (MEMS), Jan. 2024, pp. 683–686. doi: 10.1109/MEMS58180.2024.10439577.

Northeastern University

Northeastern University

At the Institute for NanoSystems Innovation at Northeastern University, Evatec's CLUSTERLINE® 200 equipped with a Multi-Source Module (MSQ 200) has been central to our exploration of co-doped nitride piezoelectrics. The platform let us validate experimental compositions using convenient 4" targets, while iterating process windows directly on 200mm wafers. In the past four years, we used this capability to explore AlScN thin films with variable Sc composition (0-42%) and thicknesses (10nm-2µm) for a variety of applications, including PMUTs for medical imaging, RF resonators for acoustic filters and sensors, metamaterials stacks, and ferroelectric memory cells.

Beyond ternary alloys, we used the MSQ to explore quaternary compositions where two elements are introduced simultaneously within the AlN lattice to further manipulate its properties. In a recent study we installed a 4" $Al_{0.45}Sc_{0.45}B_{0.10}$ cast alloy target on the MSQ to systematically map stress, texture, and surface quality versus several process parameters, and subsequently characterized the ferroelectric and piezoelectric of these B and Sc co-doped AlN thin films.

The resulting films exhibited both strong piezoelectric and robust ferroelectric responses, with d_{33} coefficients above 25 pm/V, and clear polarization switching with asymmetric coercive fields. Further work is on the way on this front, as these results validated dual doping as a promising avenue to discover new micro-acoustics materials.

The MSQ architecture materially reduced risk by proving experimental target chemistries at small sizes before committing to larger targets, and it shortened iteration cycles by enabling rapid condition trials on 200mm production wafers. We see this workflow as an important enabler for universities pursuing leading-edge MEMS and wireless devices, as well as an attractive platform for academia-industry joint R&D efforts.

Prof. Simeoni is an Assistant Research Professor at Northeastern University, affiliated with the Institute for NanoSystems Innovation and the Department of Electrical and Computer Engineering. His research centers on piezoelectric electromechanical sensing platforms for trace-chemical monitoring, optical detection, and medical imaging. He earned his B.S. in Physics Engineering (2014) and M.S. in Nanotechnologies for ICTs (2016) from Politecnico di Torino, and his Ph.D. (2021) from Carnegie Mellon University, focusing on airborne ultrasonic communication for low-power wake-up applications.

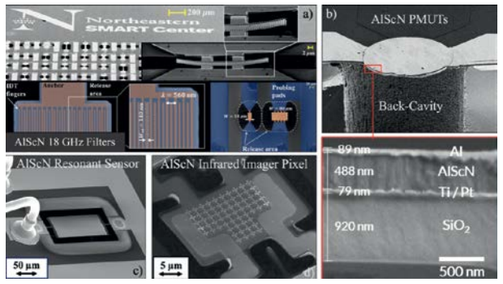


Figure 1: a) CLMR resonators for high frequency acoustic filters, b) PMUTs for intrabody ultrasonics, c) N2O resonant gas sensor, d) Infrared sensing nanoplate for imaging.

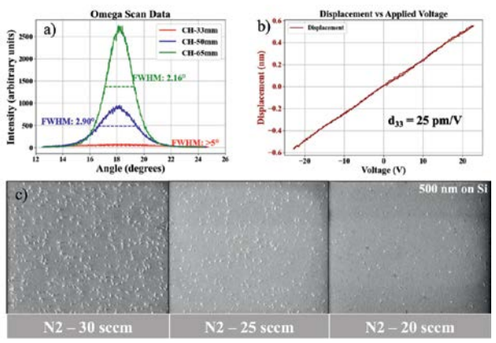


Figure 2: a) 500 nm AlScBN rocking curve vs. chuck height, b) AlScBN films DBLI d_{33} measurement, c) Surface SEM showing abnormally oriented grains vs. nitrogen flow.

UF UNIVERSITY of FLORIDA

University of Florida

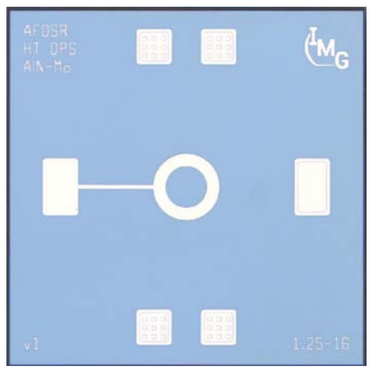
We use the Evatec tool to sputter AlN thin films and electrodes to fabricate MEMS dynamic pressure sensors. One such device, shown below, was fabricated using sequentially sputtered AlN seed layer, Mo electrode, and AlN device layer without breaking vacuum.

This capability enabled us to achieve high-quality AlN layers with a FWHM of less than 2°, maximizing our device sensitivity and performance. For similar high-temperature applications, including hypersonics and gas turbines, we will be integrating the AlN layer within NASA Glenn's SiC JFET-R process to create a first-generation monolithically integrated pressure sensor and transistor for >500°C environments in air.

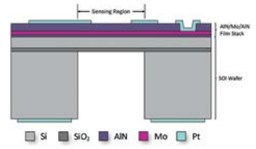
These devices will aim to measure pressure fluctuations at frequencies up to 1 MHz, enabling boundary layer characterization of hypersonic flows to improve vehicle design and direct feedback control in gas turbines to increase efficiency. Recently, we have successfully verified operation of a pressure sensor device (Figure 1a) at up to 800°C in air (Figure 1c) via electrical excitation under a digital holographic microscope (DHM), proving the feasibility of the device design at these high temperatures.

Moving forward, we will look to characterize the material properties of the device materials at high temperatures, both to improve modeling and design of the device and understand the temperature limitations and failure mechanisms of the materials for pressure sensing.

Alexander Reilly is a graduate research assistant at the Interdisciplinary Microsystems Group (IMG) at the University of Florida (UF). He graduated summa cum laude with a B.S. degree in aerospace engineering at UF in 2022 and is currently pursuing a Ph.D. degree in mechanical engineering at the same institution. His work focuses on the design, fabrication, and characterization of microelectromechanical-systems-based transducers, particularly those for high-temperature applications.



a)



b)

c)

Figure 1: a) Photograph of AlN MEMS pressure sensor (2.5x2.5 mm² die size). b) Cross-sectional schematic of pressure sensor structure. c) Device testing under probe station at 800°C in air.

Want to know more?

If you would like to learn more about Evatec's cost effective CLUSTERLINE® 200 tool configurations for R&D, simply contact your Evatec sales and service organization.

RF Filters in 2025

Choosing the right technology for performance, cost, and integration

As 5G and Wi-Fi 6E/7 reshape RF frontend design, the balance between BAW and SAW filters becomes more critical than ever. Yole Group's comparative analysis across 40+ filters reveals how OEMs optimize acoustic platforms to align performance with budget and board constraints.

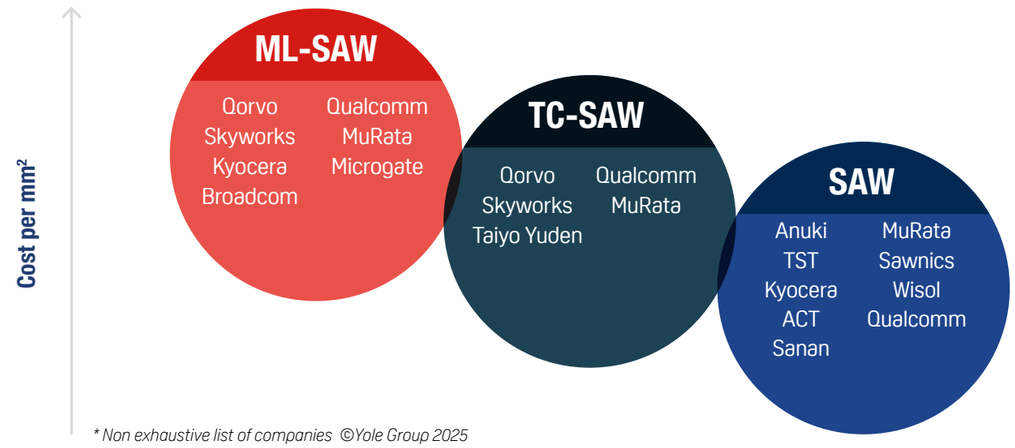
RF filters share a sizable number of components in modern RF frontend devices. In Yole's recent Status of the RF Industry 2025 report, the overall filter market is valued at $8.2 billion in 2025. The RF Filter ecosystem is diverse, with many players and filter technologies. Yole Groups reports, BAW filter Comparison 2025 and SAW Filter Comparison 2025, compared more than forty commercial filters from around twenty suppliers, including Broadcom, Murata, Qorvo, and Qualcomm, covering Automotive & Mobility, Industrial, Telecom & Infrastructure, and Mobile & Consumer equipment. Our analysis spans all mainstream surface acoustic wave (SAW) families – conventional, thermo-compensated (TC-SAW) and multilayer (ML-SAW) – and bulk acoustic wave (BAW) architectures, namely FBAR, SMR, DBAR, and XBAW. The arrival of 5G and Wi-Fi 6E/7 pushed demand for BAW filters, especially in medium- and high-band paths. FBAR still yields the best radio performance but depends on costly cavity steps and 8-inch wafer lines. SMR removes the cavity, so unit cost falls with only a modest loss in selectivity. Both flows rely on aluminum nitride layers – poly-AlN or AlN doped with niobium or tantalum – and several makers now boast electromechanical coupling by moving to aluminum scandium nitride with more than 40 % scandium. BAW devices only use Sc-AlN, not lithium niobate. Since 2022, many OEMs have trimmed FBAR and SMR usage, trading a small hit in performance for lower bills of material.

Filters manufacturers overview*

* Full analysis (company profile, physical and cost analyses)

** Non exhaustive list of companies ©Yole Group 2025*

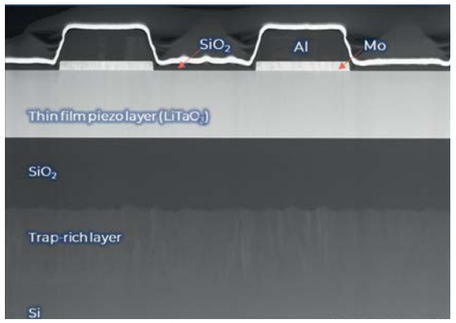
SAW filters cost comparison – by type of filter*



** Non exhaustive list of companies ©Yole Group 2025*

SAW technology remains attractive for lower frequencies and for applications where cost or board area is under pressure. It is important to note that these filters in general have a higher number of resonators per mm2 compared to BAW. Conventional SAW uses bulk lithium tantalate or lithium niobate as both substrate and piezo layer. TC-SAW improves the Thermal Coefficient of Frequency (TCF) by adding compensating films or dopants, reducing the channel drift with temperature. In ML-SAW, a thin $LiTaO_3$ or $LiNbO_3$ film is bonded to an insulating carrier – often silicon with a trap-rich layer or aluminum oxide – while bonding layer refinements cut epitaxial and thermal stress, extending reliable operation to higher bands. Taiyo Yuden and a few other suppliers use $LiTaO_3$ on Al_2O_3, while Qorvo and Skyworks have adopted SOITEC Piezoelectric-on-Insulator (POI) substrates for selected designs.

Taken together, the data shows a clear division between different technologies. Enhanced TCF and stronger bonding layers allow SAW parts to handle the low band and most of the mid bands, sometimes even reaching sub-6 GHz high-band blocks, at the lowest die cost, considering the number of resonators per filter. BAW parts, now using AlN-based thin films, are still required for the most demanding mid- and high-band 5G channels, though their cavity steps force designers to monitor cost closely. Picking the right acoustic platform, piezo film, and bonding stack for each frequency range, therefore, remains the surest way to meet performance targets without blowing the budget or the board area, which is seen in the cases of Qorvo and Skyworks where both SAW and BAW filters of different types are utilized in the same modules.



ML- SAW FIB cross section – TEM view
©Yole Group 2025

Related Yole Group's products

- *SAW Filters Comparison 2025*
- *BAW Filters Comparison 2025*
- *Status of the RF Industry 2025*
- *Automotive Radar 2025*
- *RF for Defense 2026*
- *RF for Satcom 2026*

Source: www.yolegroup.com

About the Author

Ihor Pershukov, PhD, is a Technology & Cost Analyst, Radio Frequency at Yole Group. With a deep expertise in semiconductor manufacturing, materials, and radio frequency (RF) devices, Ihor oversees reverse engineering and costing analyses. Collaborating closely with the laboratory team, he defines the objectives of the analyses and establishes methodologies to unveil the structure of RF devices. Prior to Yole Group, Ihor served as a researcher at CEA-Leti, concentrating on piezoelectric materials for acoustic device manufacturing. Ihor holds a master's degree in nanoscale engineering from École Centrale de Lyon (France) and a master's degree in applied physics and nanomaterials from Taras Shevchenko National University of Kyiv (Ukraine). He has a PhD in Materials Science from École Centrale de Lyon.

Polarization Control

of AlScN piezoelectric films in high-volume production

In a significant leap forward for piezoelectric thin film technology, Evatec has successfully developed a process for polarization control of AlScN (Aluminum Scandium Nitride) layers – marking a groundbreaking achievement for high-volume manufacturing of RF devices. Evatec's Wireless Product Marketing Manager, **Dr. Oguz Yildirim**, and Process Engineer, **Demian Henzen**, tell us more.

A new era in Wireless Communication

The next generation of wireless communication (6G) is expected to be introduced at the end of the decade. As the race to meet the technological standards for 6G intensifies, the RF frontend module is emerging as a critical component in enabling end users to access the ultra-high speeds and bandwidths that 6G promises.

While many elements of the RF frontend can be adapted for high-frequency operation, the RF filter remains the most challenging and essential part of the puzzle.

In this context, the demonstration of periodically poled piezoelectric layers marks a significant step forward. These engineered structures offer the potential to dramatically increase resonance frequencies, paving the way for high-performance filters that meet the demands of next-generation wireless systems.

Periodically poled piezo AlScN (P3F) layers represent a transformative advancement in RF filter technology. By alternating the polarization direction across the piezoelectric film, these engineered structures enable the excitation of higher-order acoustic modes, most notably the 4th thickness extensional mode (TE4). This allows resonators to operate at frequencies up to four times higher than conventional AlScN devices, reaching 17–18 GHz without reducing the film thickness and thus providing the possibility to keep quality factors and coupling coefficients [1].

"In-situ polarization control during deposition without vacuum break is now possible"

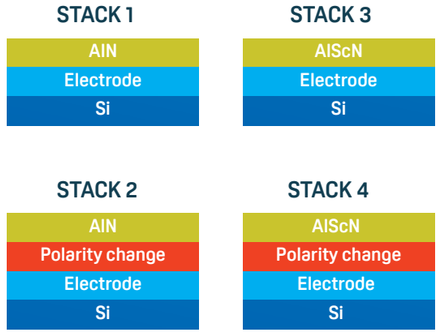


Figure 1: Stack designs for AlN and AlScN layers.

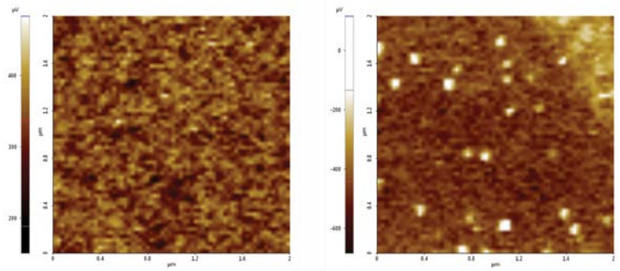


Figure 2: PFM quad images.

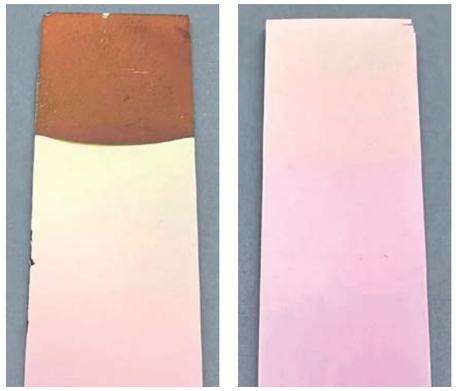


Figure 3: KOH etching results.

Polarization Control on CLUSTERLINE® 200

Using Evatec's CLUSTERLINE® 200 cluster tool platform, our process engineering team demonstrated precise control over the polarity of AlN and AlScN films through a combination of both new hardware and process developments. Particulary significant is the fact that such a breakthrough could be achieved without breaking vacuum and keeping the wafer in the same tool throughout the AlScN production process, significantly reducing the costs as compared to integration-based alternatives. This development also sits alongside our new solutions for epitaxial seed layers, hot electrodes (see LAYERS 8, 2024).

Checking the Results

Polarity control for the AlN and AlScN layers was checked by two different methods; i) KOH etching of AlN. Depending on the polarization, AlN etching rate in KOH changes significantly [2]. ii) Piezoelectric force microscopy (PFM). This technique probes the piezoelectric domains on the material and measures changes in response depending on the polarization direction (Figures 2, 3 & 4).

While these results show sucessful polarity control on the single piezo layer stack, double layer stacks with alternating polarity were also grown successfully and the device tests are currently ongoing.

[1] M. Izhar ,et al., Microsystems & Nanoengineering (2025) 11:19
[2] E. Milyutin et al, J. Vac. Sci. Technol. B 28 (6), Nov/Dec 2010

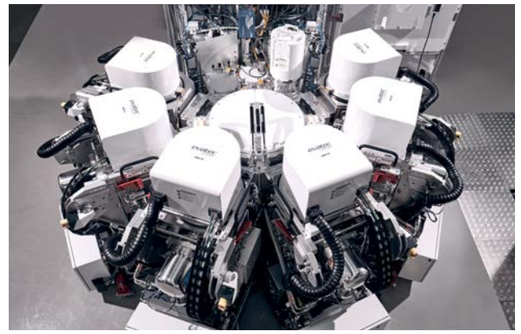
Evatec – Your long-term partner in wireless RF device technology

With over 25 years of experience in AlN-based piezoelectric layer development, and an installed base spanning North America, Europe, China, Southeast Asia, Korea, and Japan, Evatec has established itself as a global leader in RF filter technology. We are committed to pushing the boundaries of thin film technology and delivering solutions that empower our customers to innovate.

We would love to help you solve your own wireless thin film technology challenges too, so contact us today.

	AlN	AlN flipped	AlScN	AlScN flipped
STACK	AlN Electrode Si	AlN Polarity change Electrode Si	AlScN Electrode Si	AlScN Polarity change Electrode Si
RC (°)	1.29	1.44	1.63	1.49
$PFM/PFM_{(AlN)}$	1.0	-0.8	1.3	-1.1
$PFM/PFM_{(AlN)}$ Expected	1	~-1	~1.5	-1.5
Etched in KOh	Yes	No	-	-

Figure 4: Summary of the results.



CLUSTERLINE® 200.

SPOTLIGHT

About C-axis polarity control

C-axis polarity control enables RF filters working at frequencies where the frequency is defined by the thickness of the same polarity layer and not the whole thickness. For example, Figure 5a shows a conventional RF filter where the thickness defines the frequency. In Figure 5b the thickness is divided to 4 equal thicknesses which also quadruples the frequencies.

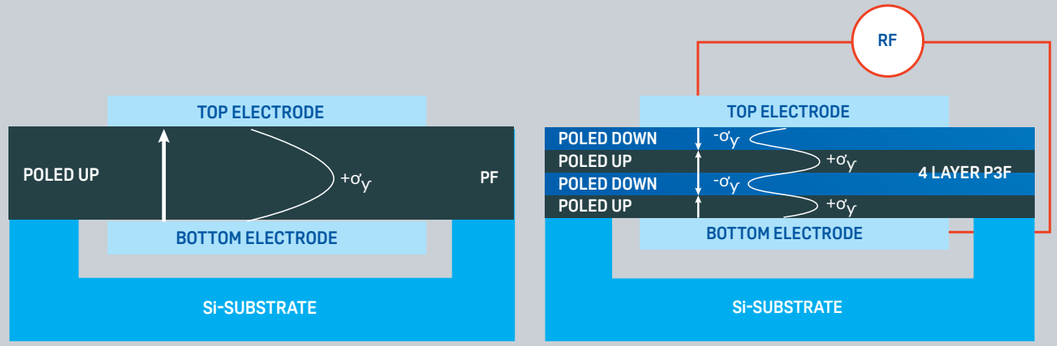


Figure 5: All about C-axis polarity control

It's all about **particle control**

As Micro LED device sizes continue to shrink to just a few or even submicron proportions, so does the manufacturing yield due to unwanted particles in the same size range generated during processing. Evatec's Process Engineer, **Nino Crameri**, and Senior Strategic Marketing Manager, **Dr. Chongqi Yu**, remind us how the basic design concept for CLUSTERLINE® 200 BPM is already a great start for reducing particles and explain how the latest Evatec process know-how can deliver the excellent particle control performance required for high-yield mass production.

The CLUSTERLINE® 200 BPM – a proven workhorse in the LED industry

When the Batch Process Module (BPM) platform concept was first developed over 10 years ago and introduced to an emerging LED industry, the goal was clear – to deliver high deposition rates, low particle levels, and excellent single layer or stack thickness control and uniformity. At that time, customers were typically handling batches with small substrate sizes of 2- or 4-inches on carriers. The engineering and process team set about designing a solution without the use of uniformity shields typically required in deposition systems to manage uniformity, bringing two immediate advantages:

- Higher basic deposition rates
- Elimination of a major source of unwanted particles

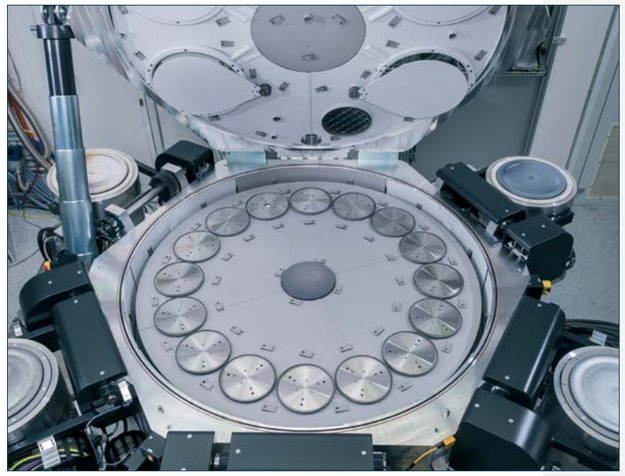
Today, Evatec's CLUSTERLINE® 200 BPM is already a proven workhorse for mass production in the LED industry. Fully automated "cassette-to-cassette" handling combined with batch module configuration processing up to 15 pieces of 8-inch substrates simultaneously make it an ideal starting concept for high throughput and low cost of ownership in mass production of Micro LED as well.

The latest generation of CLUSTERLINE® 200 BPM, integrating a turntable with individual rotating chucks, proprietary cathode magnet technology, and in-situ broadband monitoring, has become an industry-leading platform for mass production of the typical metals, TCOs and DBRs required, known for low-damage deposition on sensitive materials like GaN.

The latest results – Staying ahead of the game

Our customers need tighter and tighter particle specifications. Since the early times of 2- and 4-inch production, these days customers work more on 4- or 6-inch and we see a trend of manufacturers demanding process performance over 8-inch.

The same basic advantages of the BPM concept apply, but we need to work together with customers to optimize process technologies, especially as device sizes get smaller in the world of Micro LED. ITO is one of the most commonly specified materials. Work reported here therefore focuses on a typical, cold 40 nm ITO deposition process developed by our process specialists in collaboration with customers.



The latest generation of CLUSTERLINE® 200 BPM integrating a turntable with individual rotating chucks, proprietary cathode magnet technology and in-situ broadband monitoring.

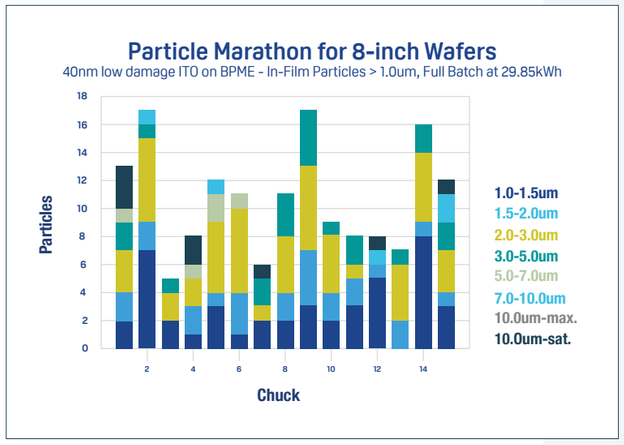


Figure 1: In-film particle levels larger than 1 micron per chuck.

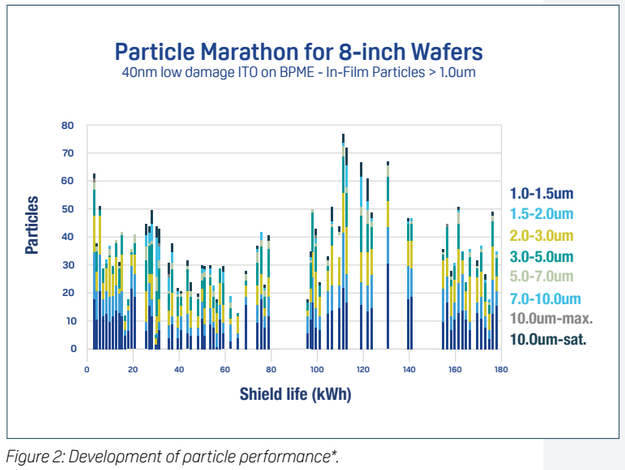


Figure 2: Development of particle performance.*

Variation from chuck to chuck

Comparison of particle levels between the 15 chuck positions of the BPM was measured as a baseline. Figure 1 shows "in-film particle levels" for particle sizes of 1 microns and above part way through target and shield life (at 30kWh) for each substrate position of the batch module turntable. We see that in-film particle levels are consistently low in the sub-20 total range across the full 8-inch substrate areas for every substrate in the batch. Compared to the complete marathon data, which is shown in Figure 2, this example shows an exceptionally low particle level. Normally, the particle count is around 40.

Variation over target/shield life

Having established no significant difference in particle performance between chucks, a single chuck position was chosen to verify the particle performance for the process over a much wider range of shield / target life. Figure 2* shows how the particle performance for chuck position 3 varies over 180kWh for particles in the same sizes range of 1 micron and above, relevant to the device manufacturer. We see that total particle numbers remain in the typical range between 20 and 80 over a whole 8-inch substrate.

Particle distribution over the wafer

Measurements were also made to verify the typical distribution of particles. To distinguish between any particles arising as a result of handling rather than during sputtering, baseline measurements were taken.

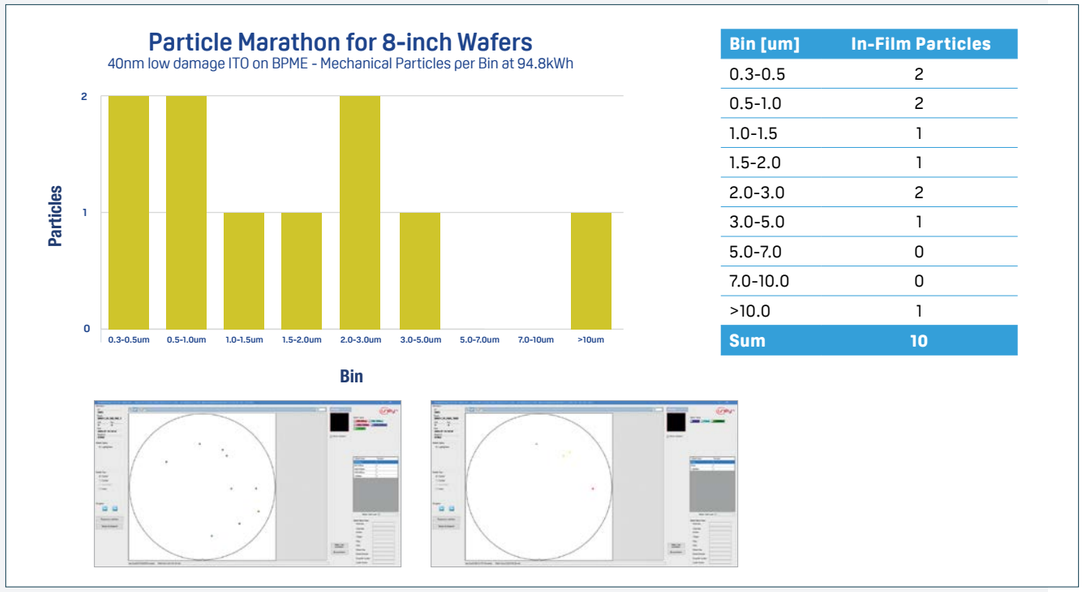
Base values

In a so-called "Mechanical Particles" test, substrates are loaded into the system within a cassette. The system is pumped, substrates are picked, loaded to the turntable, and rotated with process gases and process times as per a process recipe, but with no plasma ignition before being returned to the cassette and vented. Figure 3 illustrates the distribution after a target/shield life of 95kWh for chuck position 12 using the "precoated shields" typically used by customers to reduce shedding. As can be seen, the particle count on the substrate is very low after the mechanical test, including particle sizes starting from 300nm.

In-film particles

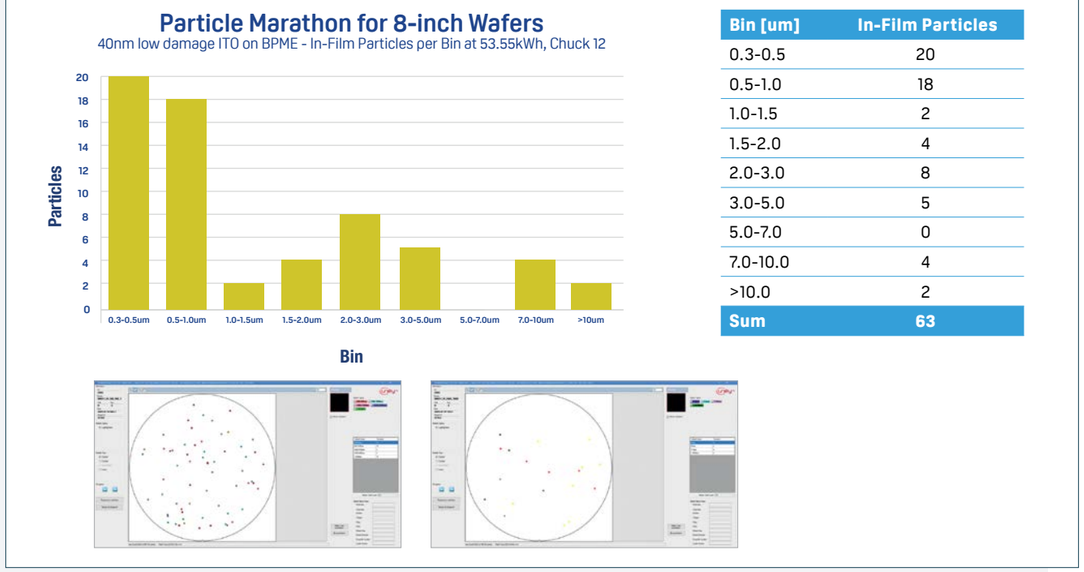
Figure 4 shows the distribution of in-film particles for the same chuck position, but at a lower shield life and also starting from 300 nm particle size.

NEXT STEPS →→



Bin [um]	In-Film Particles
0.3-0.5	2
0.5-1.0	2
1.0-1.5	1
1.5-2.0	1
2.0-3.0	2
3.0-5.0	1
5.0-7.0	0
7.0-10.0	0
>10.0	1
Sum	**10**

Figure 3: Particle distribution over the wafer for mechanical particles using typical production LED / Micro LED BKM.



Bin [um]	In-Film Particles
0.3-0.5	20
0.5-1.0	18
1.0-1.5	2
1.5-2.0	4
2.0-3.0	8
3.0-5.0	5
5.0-7.0	0
7.0-10.0	4
>10.0	2
Sum	**63**

Figure 4: Particle distribution over the wafer for in-film particles using typical production LED / Micro LED BKM.

NEXT STEPS

Whether it's metals, TCOs, or dielectrics, every customer works with different layer thicknesses, stack designs, and process conditions including temperature – and hence also different particle performance specifications. However, with more than 15 years of experience in supporting customers with sputter processes for LED, our engineers are ready to help you optimize your own specific processes.

**Footnote: Tool running continuously, processing batch after batch. A small number of outliers with high particle counts caused by random arcing events have been removed from the graph.*

Evatec LED know-how

Enabling an exciting EV future

LED technology doesn't just brighten up our world, it delivers new capabilities for the next generation of electric vehicles too. Continuous process development at Evatec is helping customers increase device performance and drive down cost of ownership in mass production of the smaller and smaller device structures on the Micro LED roadmap.

Decoration light
LED / Mini LED

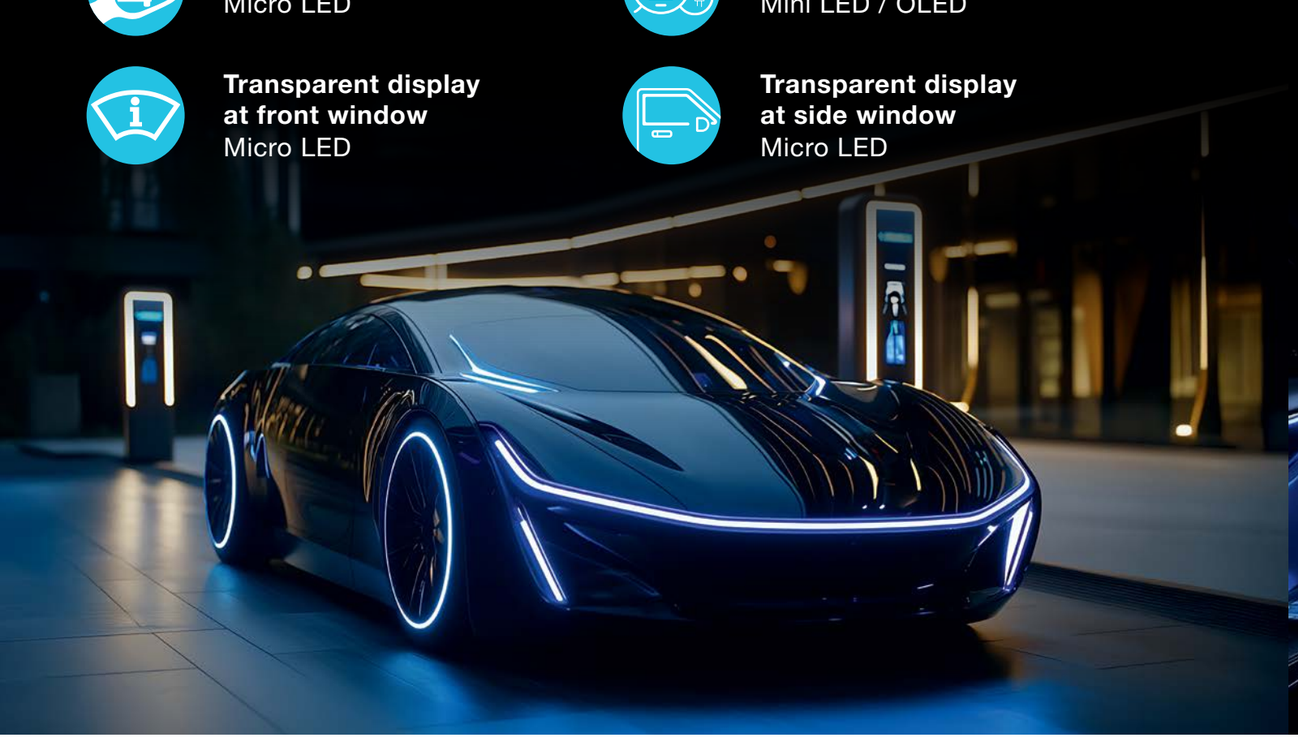
Decoration light interior
LED / Mini LED

Micro-display at the mirror
Micro LED

Dashboard
Mini LED / OLED

Transparent display at front window
Micro LED

Transparent display at side window
Micro LED



"The process team and I would love to tell you more about any of our materials or process capabilities"

Felix Hasler, Product Marketing Manager

Let Evatec support you with your process development and manufacturing roadmap

Materials know-how

TCOs
>20 years of experience in hot and cold processes for TCOs including ITO

DBRs
Custom processes reducing process times for higher throughput

Metals
High uniformity processes for contacts on 4, 6, & 8 inch

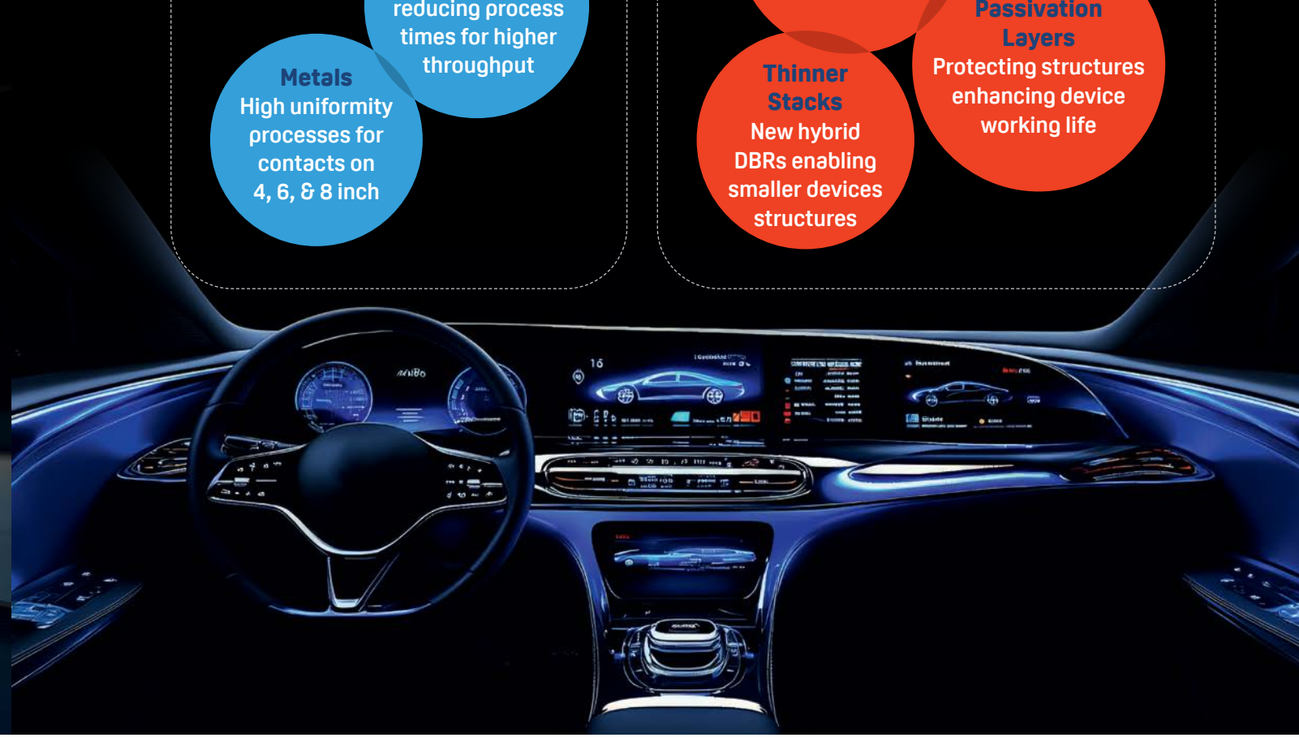
Enhancing device performance

Reducing Particles
Enabling smaller devices, increasing process yields

TCOs
Increasing light output for smaller and smaller device structures

Passivation Layers
Protecting structures enhancing device working life

Thinner Stacks
New hybrid DBRs enabling smaller devices structures



Optical monitoring

now with even “broader shoulders”

Evatec’s GSM “broadband optical monitoring” system has been supporting customers with increased precision and repeatability in optical thin film deposition for over a decade. Evatec’s Principal Scientist, **Dr. Stephan Waldner**, introduces the latest tool with extended wavelength range for direct measurement up to 1700 nm. From laser bars to bandpass filters, the broad shoulders of the new generation GSM make it an ideal choice for applications demanding the highest level of precision in the near infrared.

The new GSM 1102 – the same flexibility with more capability than ever

Just like its predecessor, the new GSM with NIR extension is designed to work in transmission or reflection measurement modes on Evatec’s range of sputter and evaporation platforms, but the addition of a second spectrometer with InGaAs detector and light-splitting hardware in combination with new firm- and hardware for data acquisition and processing enables seamless direct measurement all the way from 380nm up to 1700nm. Just like previously, customers can work in broadband, monochromatic or hybrid modes and make use of in-situ reoptimization for “on-the-fly” tuning in production (Figure 1).

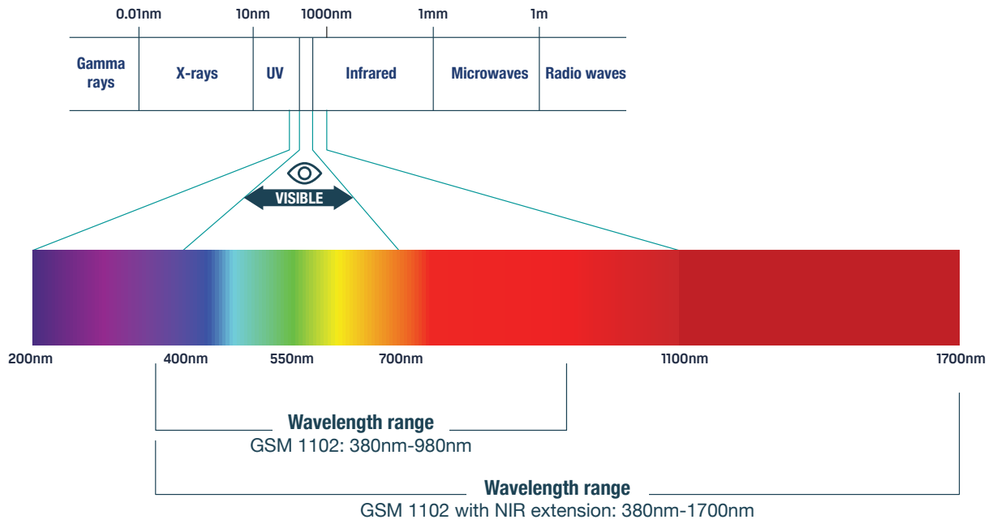


Figure 1: Comparison of the wavelength ranges of the GSM 1102 without (380 – 980nm) and with the NIR extension (380 – 1700nm).

Applicable Coating Tools	Measurement Modes	Monitoring Algorithm	Monitor Substrate
• BAK evaporation • CLUSTERLINE® 200 BPM • CLUSTERLINE® 200 PECVD • SOLARIS®	• Transmittance • Reflectance	• Broadband monitoring • Monochromatic monitoring • Hybrid mode (broadband/mono) • In-process reoptimization	• Direct monitoring on substrate • GTC1100 test glass changer on BAK • GTC621 test glass changer on BAK

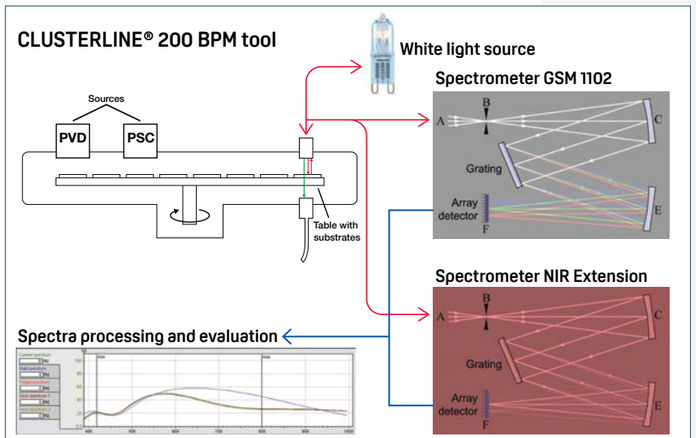


Figure 2: Schematic of the GSM 1102 with NIR extension integrated on a CLUSTERLINE® 200 BPM tool.

"The NIR extension is also available for retrofit on an existing GSM 1102"

Case studies

Here we present some typical results for sputter deposition processes carried out on Evatec's CLUSTERLINE® 200 equipped with batch process module (Figure 2). The GSM was working in broadband mode measuring directly on the substrate in reflection at each rotation of the turntable every few seconds.

The screenshot in Figure 3 during a test run of a simple 2 layer process for Ta_2O_5 then SiO_2 on a quartz glass substrate illustrates what users see on the Graphical User Interface (GUI) during deposition.

Whilst in this case the defined monitoring range was 420nm to 1640nm, the full reflection spectrum was measured over the entire 380nm to 1700nm at every table rotation (3s).

The lower part of Figure 3 shows the noise-free, continuous spectrum measured over the full wavelength range (current spectrum, green) in excellent agreement with the simulated spectrum (theoretical end spectrum, brown). The Figure of Merit (FoM) curve over time in the upper right is perfectly smooth, indicating the stability of the reflection measurement.

Results

Three typical coating designs for the NIR range were chosen: A broader as well as a very narrow bandpass filter, and an antireflective coating were deposited on a CLUSTERLINE® 200 BPM tool equipped with GSM 1102 and NIR extension using Ta_2O_5 and SiO_2 as coating materials and evaluated afterwards using spectrophotometry.

1. Design 1: 33-layer Bandpass filter at 1310nm with 40nm bandwidth
The transmittance measurements of two coating runs show an excellent reproducibility as well as agreement with the theoretical design spectrum.

2. Design 2: 27 layer bandpass filter at 1530nm with 3nm bandwidth
The high resolution and low noise level of the spectrometers in the GSM 1102 and the NIR extension allow accurate monitoring of even very narrow bandpass filters. Note that 3nm bandwidth corresponds to as little as 0.2% of the center wavelength 1530nm.

3. Design 3: 4-layer AR design at 1550nm
Still, the most widely used optical coating designs are antireflective coatings. The 4-layer AR coating deposited on both sides of a quartz substrate leads reliably to transmissions >99.95% at 1550nm.

Why not upgrade your capabilities now? The new GSM extension is available not only on new tools but also as part of a retrofit package for existing GSM 1102 users. If you would like to know more, simply contact your local Evatec sales and service organization.

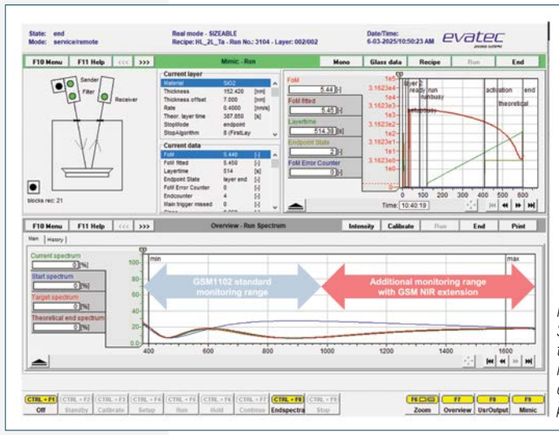


Figure 3: Screenshot of the GSM user interface during a deposition process.

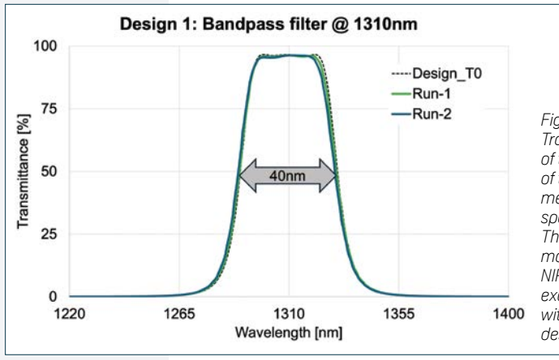


Figure 4: Transmission spectra of two coating runs of the bandpass filter measured ex-situ in a spectrophotometer. Thanks to the direct monitoring with the NIR extension, an excellent agreement with the theoretical design is achieved.

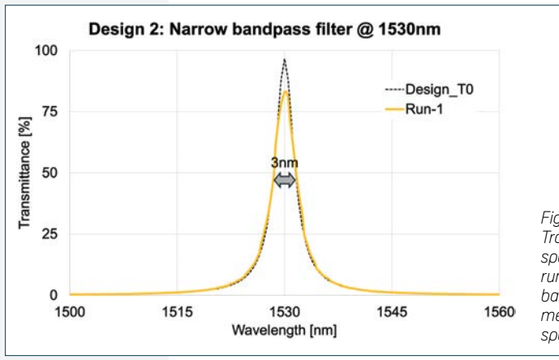


Figure 5: Transmission spectrum of a coating run of the narrow bandpass filter measured ex-situ in a spectrophotometer.

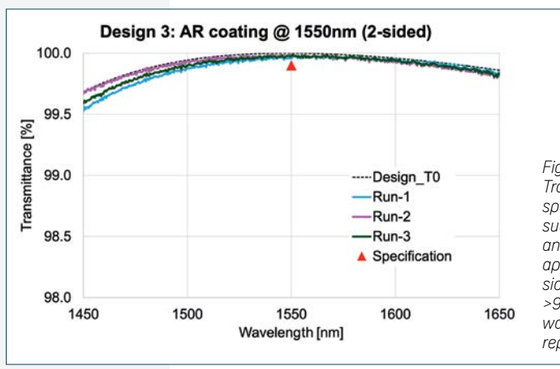


Figure 6: Transmission spectra of three substrates with an anti-reflective coating applied on both sides. Transmission >99.95% at 1550nm was achieved reproducibly.

Quantized Nanolaminates

– the next step on the road to mass production

Nanolaminate technology offers users the potential to “tailor” thin film production processes in different ways according to their priorities. For some it will be thin film stacks with enhanced optical performance, for others it could be the desire for a “wider” production window, and for others it could be achieving mass production of films only possible until now by IBS at much higher throughput and lower costs. Evatec’s Principal Scientists, **Dr. Silvia Schwyn Thoeny** and **Dr. Stephan Waldner**, report the latest progress on nanolaminate technology through two different cases on CLUSTERLINE® 200 BPM in collaboration with partners from RhySearch and EMPA.

Figure 1a: Evatec CLUSTERLINE® 200 BPM deposition tool opened for service

Production platform set-up

CLUSTERLINE® 200 BPM is a magnetron sputter deposition tool equipped with automatic substrate loading from cassette-to-cassette using a vacuum robot. It can be configured with up to four sputter sources, a plasma source (PSC), plasma emission monitoring (PEM), and an in-situ optical monitoring system with broadband and monochromatic capability.

Figure 1a shows the deposition tool with sputter and plasma sources swung out to service position and the process chamber lid opened. 15 substrates of 200 mm diameter are placed on a turn table. Each substrate is additionally rotating to achieve excellent thickness uniformity without using shaper masks.

When depositing Ta_2O_5/SiO_2 Quantized Nanolaminates (QNL), both sources are running simultaneously (Figure 1b). Both materials are sputtered from metallic targets and oxidized near the sputter target, controlled by the PEM. During one rotation of the table, each substrate receives a thin Ta_2O_5 layer and a thin SiO_2 layer when passing below the respective sources. The thickness of such a layer pair can be adjusted by the table rotation speed, whereas the ratio between high-index and low-index material is defined by the sputter powers (see Figure 2). The PSC is used to pre-condition the substrates or to influence layer stress. Figure 1c) shows a transmission electron microscopy (TEM) analysis of a nanolaminate consisting of Ta_2O_5 (black, approx. 1.35nm thick) and SiO_2 (white, approx. 2.18nm thick) layers.

The flexibility of the tool allows deposition of QNL layers consisting of a variety of materials, e.g. amorphous Silicon (a-Si) and SiO_2. To deposit multilayer optical interference coatings with QNL layers, the process sequence simply consists of the standard high- or low-index material deposition steps and the QNL layer steps.

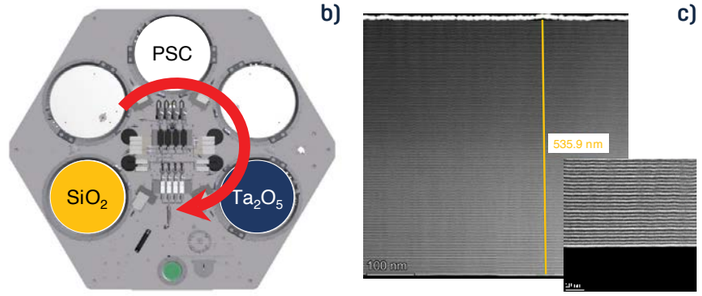


Figure 1: b) Schematic for deposition of Ta_2O_5/SiO_2 QNL; c) TEM analysis of a Ta_2O_5/SiO_2 QNL.

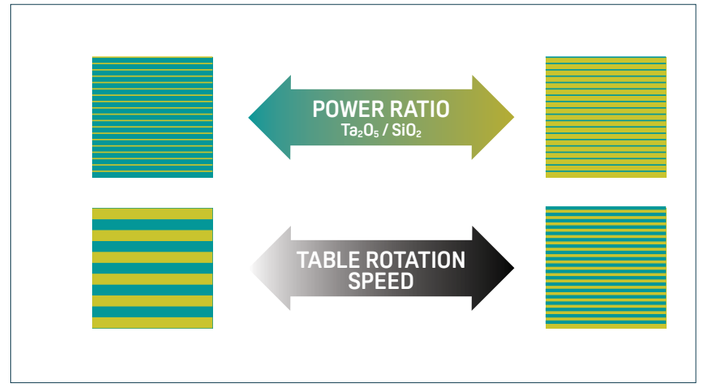


Figure 2: a) Changing the ratio of the power applied to the sputter sources allows tuning of the material composition and therefore the overall refractive index of the QNL. b) By changing the rotation speed of the substrate table, the thickness of a layer pair of the QNL deposited during each rotation can be adjusted without changing the overall material composition.

Why Nanolaminates?

- Improved process stability
- Improved film performance
- Lower cost of ownership in production

Antireflection coatings – A case study

Background
In the early times of optical interference coatings, traditional antireflection (AR) coatings were composed of quarter wave optical thickness layers of three different materials. With the advent of sophisticated coating design programs, antireflection designs with optical thicknesses departing from quarter waves could be designed.

Macleod showed with the concept of "equivalent layers" that any intermediate index layer could be replaced by three layers of high- and low-refractive-index material. This approach typically results in some thin layers, which are very sensitive to small thickness errors and reduced yield. Nevertheless, with the advent of powerful process and optical thickness control, the two-material approach became less complex than handling three materials and thus the two material AR became standard.

In this study, we revisited this assessment using QNL. The effective refractive index of the nanolaminate is defined by the thickness ratio of the high- and low-index material in the nanolaminate layer sequence and can be set to any value within the boundaries of the high- and the low-index material, which in this study are SiO_2 and Ta_2O_5. (Note: In the context of this work, the QNL are not used for the quantization effect and the related shift of the absorption edge, which was shown to occur at individual layer thicknesses of less than 2 nm).

The design study presented here compares antireflection coating designs using QNL layers with intermediate effective refractive index to standard designs using SiO_2 and Ta_2O_5. Compared to the standard design, the QNL approach was expected to show reduced average reflection and improved stability to thickness errors, and would therefore be expected to improve the production yield.

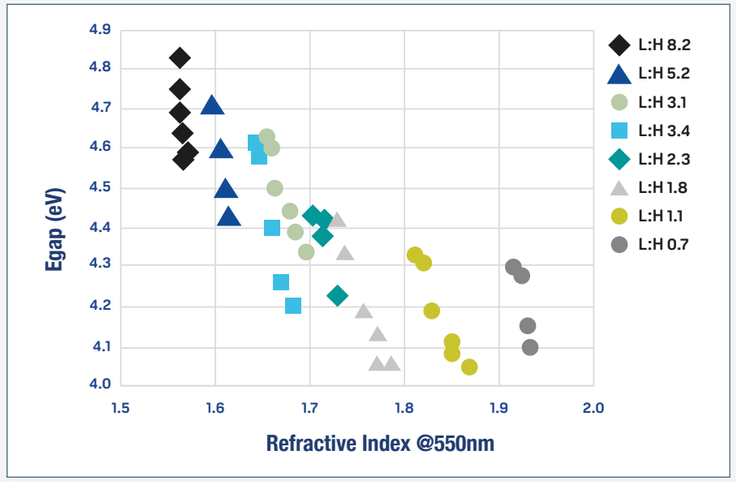


Figure 3: Dependance of gap energy to refractive index

Experiments to develop QNL with a wide range of refractive index
A series of experiments was performed varying the ratio of the thicknesses of Ta_2O_5 to SiO_2. The power on each source was varied as a main parameter. The deposition rates of the nanolaminate layers were typically higher than for the corresponding single material layers, since nanolaminates are sputtered from two sources.

For each H:L ratio, a set of deposition runs with different table speeds was deposited in order to vary the thickness of the individual nanolaminate layers. Typically, table speeds of 1.5 / 3 / 4.5 / 6 / 9 / 12 / 15 s/pass were chosen with the fastest speed of 1.5s/pass leading to the thinnest layers. Figure 3 shows the relation between band gap energy and refractive index.

The gap energy is shifted towards higher energies when the Ta_2O_5 layers become thinner and thereby confirms the occurrence of the quantization effect in the layers. Important in the current context is to note, however, that the effective refractive index can be tuned in a very wide range between the indices of SiO_2 to Ta_2O_5.

Furthermore, the effective refractive index within a series of specific L:H ratios, i.e. average composition, remains in a narrow band with a small trend to lower index for thinner layer pairs.

Design study
Based on these results, three designs of an antireflection coating for the visible part of the spectrum were evaluated. Two of them used refractive indices with intermediate values, while avoiding thin layer thicknesses. Figure 4 shows a comparison of a standard design using SiO_2 to Ta_2O_5 and two alternative designs using intermediate indices based on QNL, one with 3 layers and one with 7 layers. It can be seen from the diagram, that already the 3-layer design leads to a similar average reflection in the range of 450-650nm than the standard design and the 7-layer design improves the performance even more.
Figures 5 a, c & e show the index profiles of the three designs. The 6 layer Ta_2O_5-SiO_2 AR coating contains two very thin layers, which is typical in this type of design. The 3 and 7 layers in the mixed designs have more equal physical thicknesses. As mentioned in the introduction, it is the goal of this work to investigate whether the use of QNLs with intermediate effective refractive index offers enhanced stability against production variations. Thus, the designs were tested by introducing cumulative errors of 2 nm absolute and 1% random RMS deviation in thickness, and of 1% RMS refractive index variation for each material and layer. It can be seen from Figure 5 b, d & f that designs with intermediate index would lead to markedly narrower deviations for the 3 layer and also the 7 layer design.

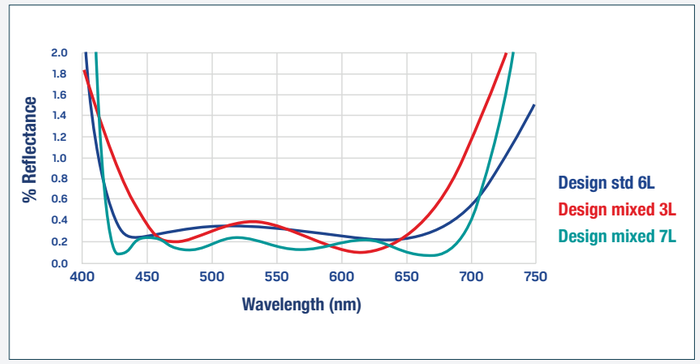


Figure 4: Antireflection designs for a standard 6 layer SiO_2 - Ta_2O_5 and 3 and 7 layer designs using QNL.

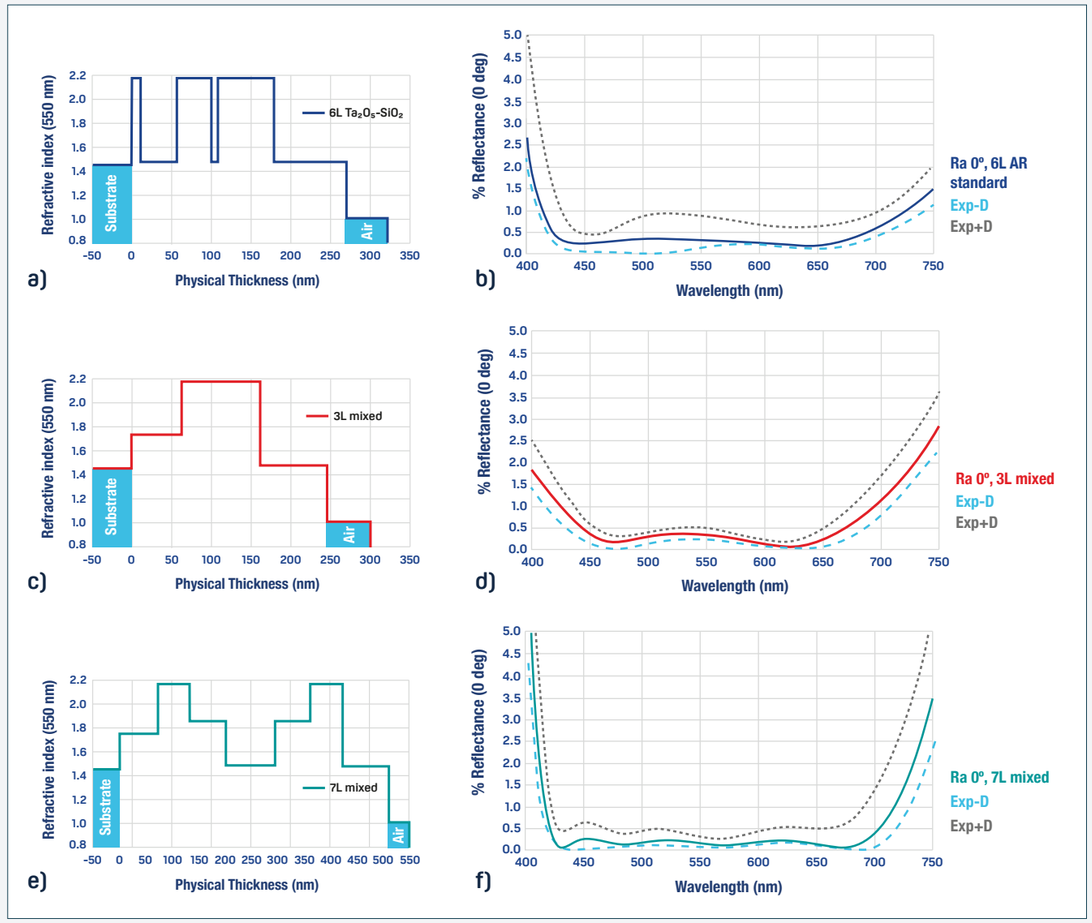


Figure 5: a,c,e) Refractive index profile of 6 layer SiO_2 to Ta_2O_5 and 3 and 7 layer designs using QNL, b,d,f) expected deviation (1σ) of the respective designs due to thickness and refractive index deviations.

Experimental results

Figure 6 shows the actual experimental results achieved on CLUSTERLINE® 200 BPM for the 3 AR coating designs. In each case, the tool produced 10 process runs which were also non-consecutive to test the process robustness in conditions closer to the real world. For comparison of the stability and performance of the produced coatings, the average deviation between the reflection spectra as well as the average reflection over 430 to 680nm was calculated.

Figure 7a shows that both designs using QNL lead to a significantly lower deviation than the standard design. The average reflectance in 7b is almost identical for the standard and the 3 layer mixed design, whereas a much lower value is achieved with the 7 layer mixed design.

As expected, we see the following important results using QNLs:

1. Lower average deviation for intermediate-index AR designs
2. Lower average reflectance for 7 layer intermediate-index design

This confirms the potential of using intermediate index designs to lower the sensitivity to process deviations relative to standard designs, increasing production robustness or offering the possibility to tailor properties such as angular shift or polarization.

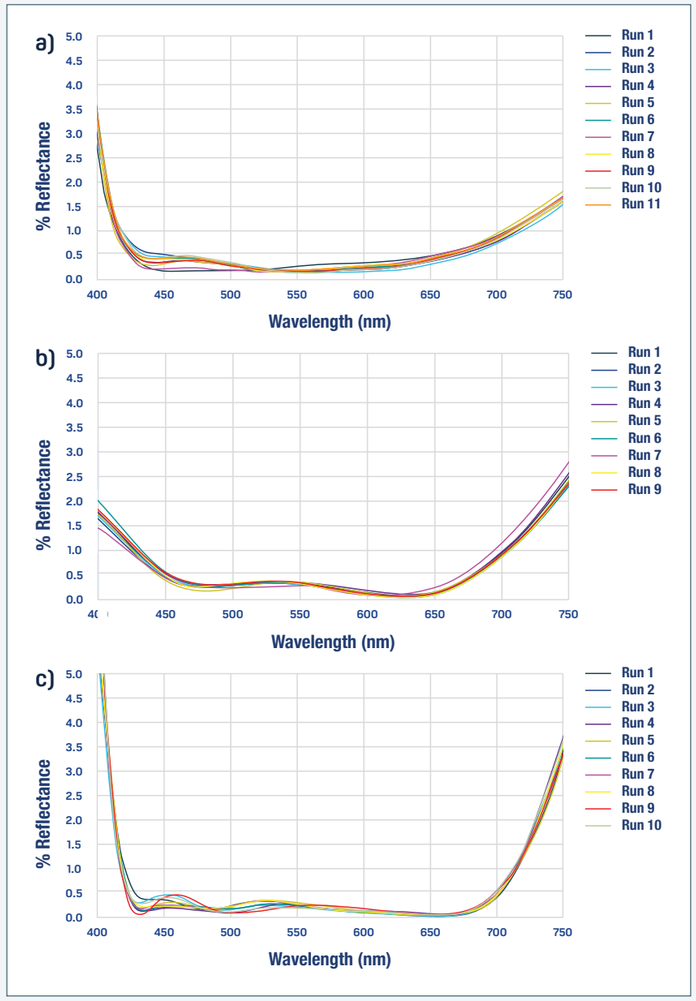


Figure 6: a) Reflection spectra of repeated runs of the standard 6 layer design, b) of the 3 layer design with a QNL material, c) of the 7 layer design with two QNL materials.

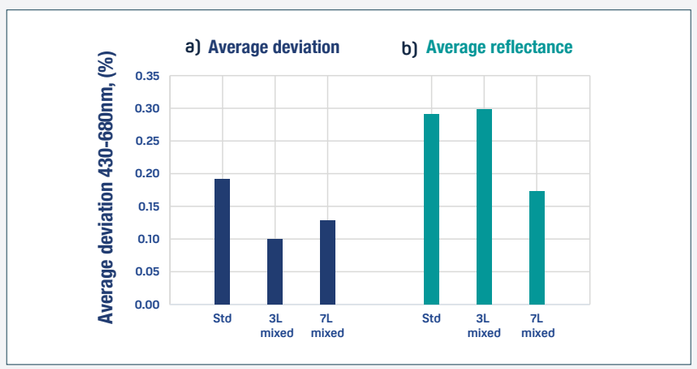


Figure 7: Experimental results comparison – standard vs intermediate index designs: a) average deviation between runs, b) average reflectance over 430…680nm.

LASER Mirrors – A case study

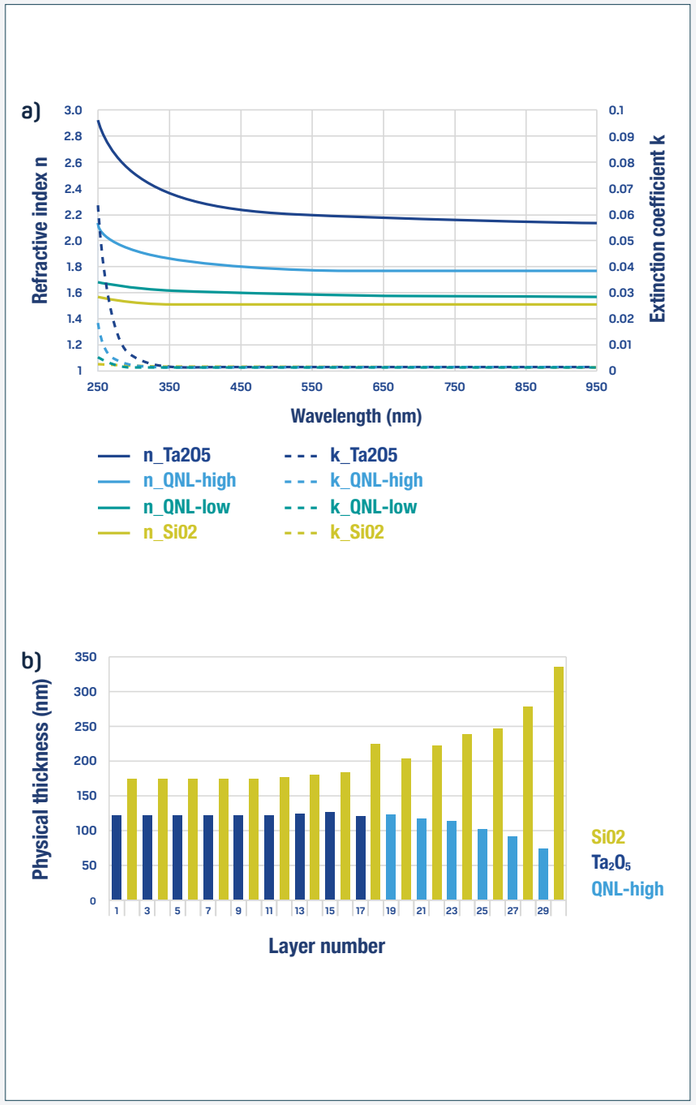


Figure 8: a) Refractive index dispersions SiO_2, Ta_2O_5, and of two Ta_2O_5/SiO_2 QNLs; b) Design thicknesses of a mirror for 1030nm consisting of Ta_2O_5, SiO_2 and a QNL material.

Background

Nanolaminates exhibit a higher band gap energy than what would be expected from a homogeneous mixture of the high- and low-index material. This increased band gap leads to a shift of the absorption edge to shorter wavelengths, as well as to a higher laser-induced damage threshold (LIDT). QNLs therefore enjoyed growing interest in the optical thin film community, but work was mainly performed using ion beam sputtering or atomic layer deposition with relatively low deposition rates and substrate loading capacity. However, if comparable performance of the coatings can be reached, magnetron sputter could offer much reduced cost of ownership for production of QNLs.

In this study, we investigated how multilayer coatings that contain QNLs could be produced on the CLUSTERLINE® 200 BPM sputter deposition tool and compared fs-LIDT results of mirrors for 1030 nm with those produced by standard sputter and IBS techniques.

Design study

QNLs can be used in a multilayer design like an additional material of intermediate refractive index. Figure 8a shows the refractive index dispersions determined from spectrophotometric measurements of two different QNLs, along with the SiO_2 and Ta_2O_5 refractive indices. These material properties can then be used like standard materials in multilayer designs.

As an example, Figure 8b shows the layer thicknesses of a 30 layer mirror for 1030nm at 0° angle of incidence (AOI). For layers 1 to 18 Ta_2O_5 and SiO_2 are used to form the base mirror, whereas QNL and SiO_2 are used for the remaining layers to make use of the postulated higher laser damage threshold of the QNL material. This is justified because

high electric field amplitudes are expected near the mirror surface. Additionally, thicknesses were adjusted to lower the E-field amplitudes in the QNL and Ta_2O_5 layers.

When coating the various designs, the thicknesses of the layers were controlled by optical monitoring. The in-situ optical monitoring GSM 1102 equipment measures reflection on a defined substrate at every rotation of the substrate table. Therefore, the monitoring "sees" an additional layer pair of the QNL with every measurement. The measured reflection spectra agree very well with the simulations based on the determined refractive index of the QNL. Figure 9a shows the spectra measured by the optical monitor at the start and end of the standard Ta_2O_5 layer 17, whereas 9b shows the corresponding spectra for the QNL layer 19. This illustrates that the changes in the reflection spectra from start to end of the layers are significant, which allows for precise layer termination by optical monitoring. Therefore, no specific adaptation of the optical monitoring process is required for the QNL layers.

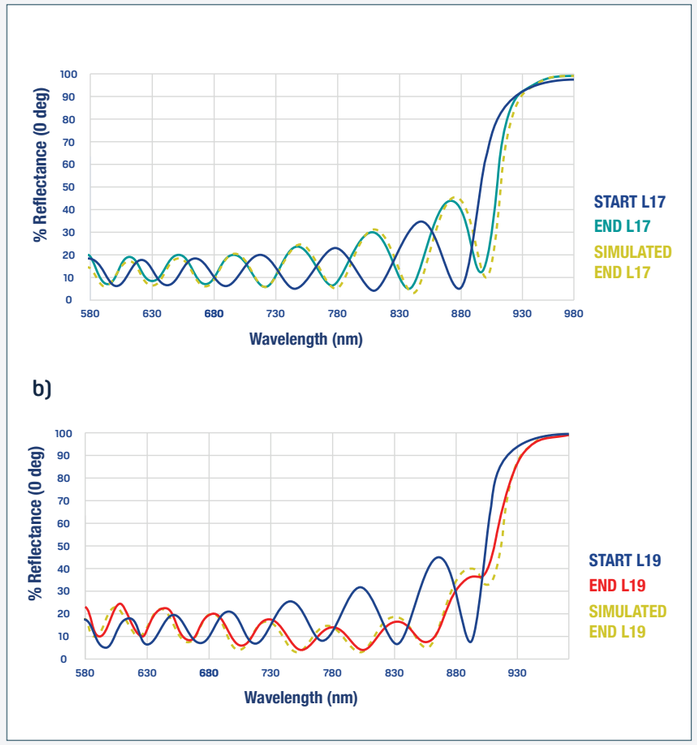


Figure 9: a) Optical monitoring spectra at start and end of the Ta_2O_5 layer 17; b) Start and end spectra of the QNL layer 19.

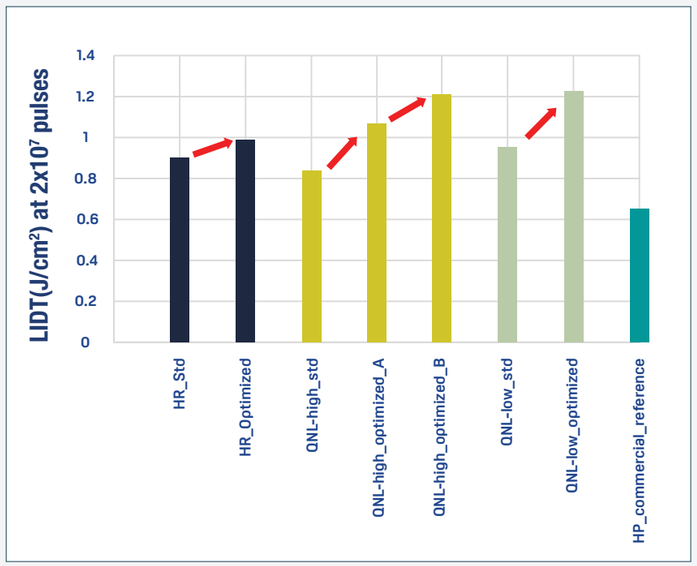


Figure 10: Femtosecond LIDT at 2 × 10^7 pulses for different mirrors for 1030nm. The arrows indicate the improvement due to the E-field optimization.

Experimental Results

Inspired by the contest of the 2024 SPIE Laser Damage Conference, a series of mirrors for 1030nm at 0° AOI with and without QNL layers were designed, deposited, and characterized. For each material combination, "std" designs composed of quarter-wave layer thicknesses were set up, as well as "optimized" designs, where the layer thicknesses were adjusted to reduce the electric field amplitudes in the higher-index layers close to the mirror surface. The "HR" designs consisted of Ta_2O_5 and SiO_2 layers only, whereas the "QNL-high" designs used Ta_2O_5 for the first part of the design and QNL with high-index for the remaining part. See Figure 8b for layer sequence and thicknesses. Accordingly, "QNL-low" used the lower-index QNL material.

These multilayer designs were deposited as described in the previous sections and then submitted to femtosecond laser damage testing at the LIDT facility at RhySearch. The test conditions were 1030nm laser wavelength with 300fs pulse duration, 200kHz repetition rate, and an effective beam diameter of 32µm. LIDT was determined for 2 × 10^7 pulse repetitions.

Figure 10 summarizes the LIDT results. The fabricated mirrors achieved an LIDT in the range of 0.83 to 1.23 J/cm². For all material combinations, the "optimized" designs reach higher LIDT than the "std" quarter-wave designs. The two best results are the mirrors which contain QNL layers, whereas the Ta_2O_5 / SiO_2 mirror "HR" does not exceed 1.0 J/cm². For comparison, a commercially available ion-beam sputtered mirror for high power fs-laser applications was included in the test. It reached an LIDT of 0.66 J/cm², i.e. significantly lower than all other samples.

Based on these results, we conclude that tuning the deposition parameters of the CLUSTERLINE® 200 BPM allows for successful adjustment of the refractive index of the QNL and for optimization of the bandgap shift. The QNL layers can be incorporated into multilayer designs using the standard tools for characterization, design, and optical monitoring. LIDT testing of the mirrors showed an excellent performance of the designs containing QNL layers.

NEXT STEPS

We continue to collaborate closely with our partners to refine processes on 6" and 8" substrates. Interested in exploring nanolaminate technology with us? Reach out to your local Evatec sales and service team to discover how we can support your next innovation.

Acknowledgements

The work reported here is a compilation of two studies first reported at the Optica Optical Interference Coatings conference, Tuscon, Arizona in May 2025 https://www.optica.org/events/topical_meetings/optical_interference_coatings with additional material added since that time.

Those original studies were published in collaboration with additional authors from Empa Laboratory for Mechanics of Materials and Nanostructures, Feuerwerkerstrasse 39, 3602 Thun, Switzerland, and RhySearch, Werdenbergstrasse 4, 9471 Buchs, Switzerland. We would like to thank Manuel Bärtschi, Fabian Steger, Daniel Schachtler, Christoph Sturzenegger from RhySearch and Xavier Maeder and Vivek Devulapalli from Empa for their kind permission to reuse extracts of those first OIC publications within this article.

Empa Materials Science and Technology

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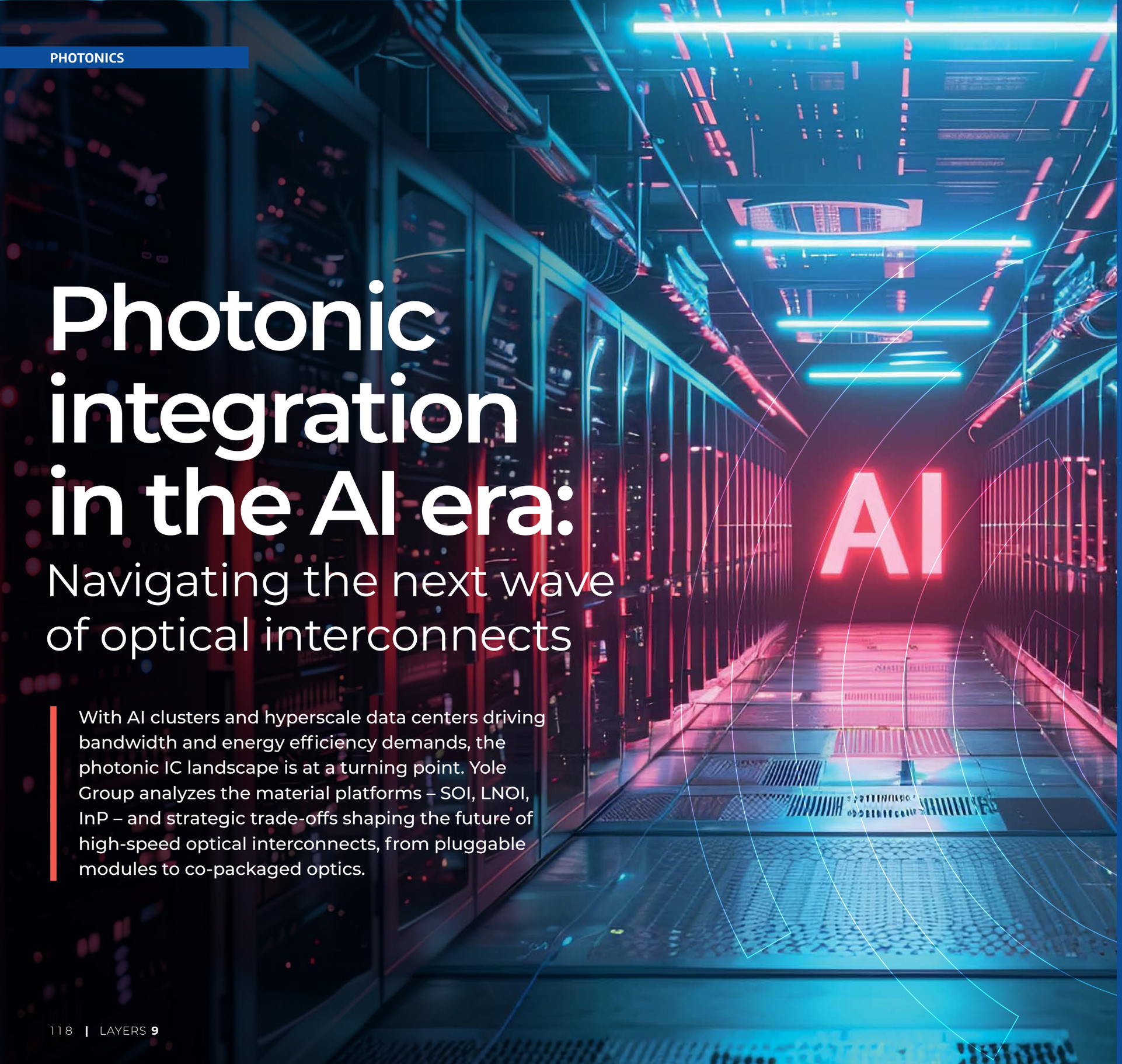
Photonic integration in the AI era:

Navigating the next wave of optical interconnects

With AI clusters and hyperscale data centers driving bandwidth and energy efficiency demands, the photonic IC landscape is at a turning point. Yole Group analyzes the material platforms – SOI, LNOI, InP – and strategic trade-offs shaping the future of high-speed optical interconnects, from pluggable modules to co-packaged optics.



YOLE Group

In the rapidly evolving optical interconnects market, demand for scalable, high-speed, energy-efficient modules is surging, fueled by AI clusters and hyperscale cloud data centers. Although CPO promises ultra-low power and high density, many network operators and system vendors continue to favor pluggable modules for their proven cost-effectiveness, easy front-panel access, and multivendor interoperability.

PICs are specialized chips that integrate various optical components, like lasers, modulators, and detectors, onto a single substrate, enabling the manipulation of light within a compact footprint. Silicon is one of the most widely used materials for photonic integration, especially in data center and telecom applications. Silicon photonics (linked to a SOI material platform) leverages CMOS-compatible processes, enabling large-scale, cost-effective manufacturing.

It's ideal for integration with other materials for functions like modulation and detection. Silicon photonics is often combined with InP material for hybrid or heterogeneously integrated light sources. Widely used hybrid integration will work for 100G/lane and should also work for 200G/lane, but beyond that, there are challenges that must be overcome.

To achieve 400 Gbps per lane and beyond, the industry is exploring deeper integration of exotic materials for modulators, detectors, and waveguides on SOI substrate. The heterogeneous integration of not only a III-V laser, but also exotic materials, adds complexity that lowers the yield and raises the cost of the PIC and delays the time to market. It is essential to design new PICs that meet the future bandwidth requirements and make them commercially viable.

Two strategic pathways: Higher speed per lane vs. Slow and wide optics

Higher speed per lane

Higher per-lane rates enable per-port Ethernet speeds of 3.2 Tbps (and beyond), while delivering roughly 20–30% power savings and a 50% reduction in laser count. Fewer lasers lower capex, simplify supply chains, and shrink operational expenses for cooling and power delivery. This strategy brings new opportunities for additional platforms into play. LNOI and InP are more straightforward solutions for future high-speed links due to intrinsic material properties.

LNOI benefits from excellent electro-optic modulation efficiency, ideal for ultra-high bandwidth applications targeting LPO, LRO, and coherent-lite pluggable optics. All TFLN/LNOI suppliers in this field have developed TFLN PICs which will compete with SOI in the same applications. However, it will be challenging at the beginning due to the high cost and limited mass production.

InP stands out for its ability to integrate active photonic components directly into the chip. This minimizes the need for complex assembly, though the technology currently incurs high costs and remains at a low production volume. InP could become a formidable competitor to SOI and LNOI by 2030, especially for coherent-lite applications.

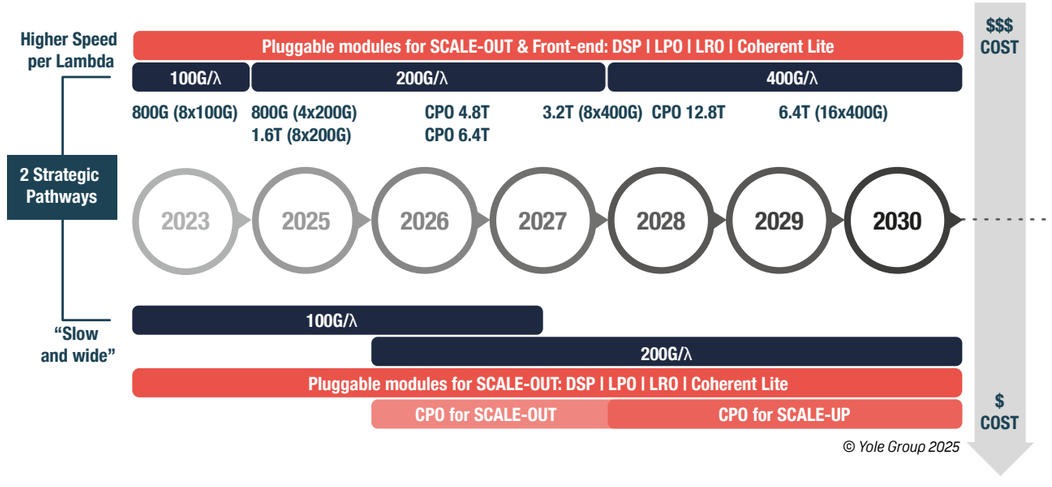
Slow and wide optics

The yield of new materials integration on an SOI platform, as well as large-scale manufacturing of LNOI or InP platforms, may not meet cost expectations by 2028.

The “slow & wide” model unlocks simpler electronics, mature optical components, and high port densities. A high radix enables more lanes at lower speeds and cheaper modulators. As the integration of silicon photonics matures, expect the radix to climb even higher (16, 32, or more) to hit multi-terabit pluggable modules as well as CPO engines.

Slow and wide” optics hit high aggregate bandwidth by keeping each lane modest in speed while multiplying lanes across fibers or wavelengths, which eases analog design, improves signal integrity and margins, can lower per-lane power, reduce DSP complexity and latency, leverage mature, lower-cost components (especially for short reach), and often help yield and reliability. However, the approach pushes problems elsewhere: you need many more SerDes and fibers, which strains package pins, retimers, and co-packaging budgets and front-panel density. Slow and wide shines for short-reach intra-rack/row links and latency-sensitive AI/ML clusters using simple NRZ/PAM with light – ideal for CPO systems.

Two pathways toward future high bandwidth datacom optics



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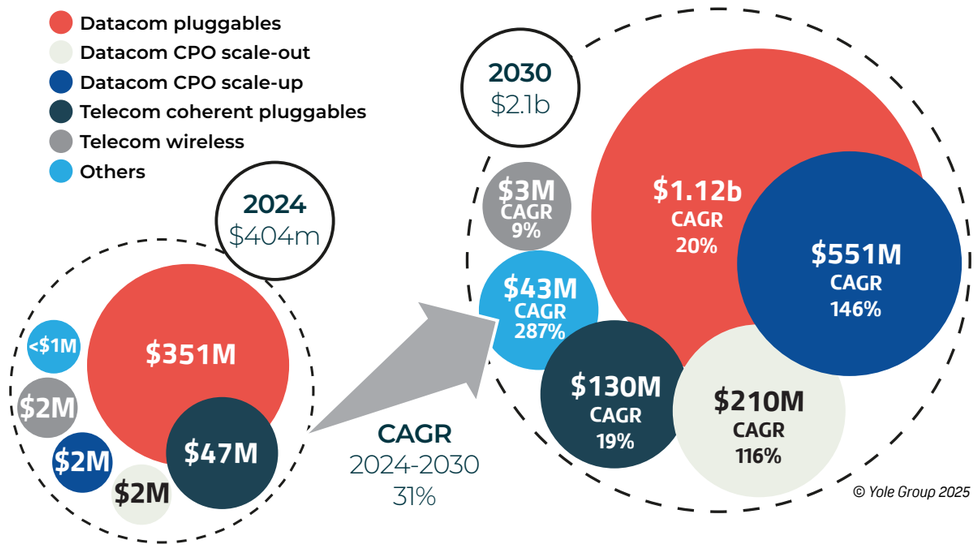
Related Yole Group’s products

- *Optical Computing 2024*
- *Silicon Photonics 2025 - Focus on SOI, SiN, LNOI & InP Platforms*
- *CISCO - QDD-400G ZR-S Optical Transceiver Die Analysis*
- *Co-Packaged Optics for Data Centers 2025*
- *Optical Transceivers for Datacom and Telecom 2026*
- *Photonics Packaging 2026*
- *Quantum Technologies 2026*

Photonic integrated circuit market

Pics (dies) revenue growth forecast: by technology platform (2024 vs. 2030)



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Looking ahead

As data center operators demand ever higher bandwidth per watt and lower total cost of ownership, the battle among SOI (plus TFLN/BTO/polymer), LNOI, and InP platforms will intensify. Pluggable modules, whether IM-DD or coherent-lite, will continue evolving in speed, integration, and power efficiency. Meanwhile, CPO designs will need to demonstrate robust performance and ease of deployment before replacing pluggables in mainstream systems. The next five years will determine which material platform delivers the optimal balance of cost, power, and performance.

The silicon PIC (dies) market was worth $404M in 2024 and is forecast to grow to more than $2.1B in 2030 at a 31% CAGR2024-2030. This growth will be driven mainly by high-data-rate pluggable modules for increased fiber-optic network capacity. Additionally, projections of rapidly-growing training dataset sizes show that data will need to use light for scaling ML models using CPO in AI clusters.

About the Author

Martin Vallo, PhD, is Senior Technology & Market Analyst, Photonics at Yole Group. Martin specializes in optical communication and semiconductor lasers within the Photonics & Sensing activities at Yole Group. With 12 years’ experience in semiconductor technology, Martin is currently involved in the development of technology & market products as well as the production of custom consulting projects.

Prior to his mission at Yole Group, Martin worked at CEA (Grenoble, France), where he focused on the epitaxial growth of InGaN/GaN core-shell nanowire LEDs by MOCVD and their characterization for highly flexible photonic devices.

Martin graduated from the Academy of Sciences, Institute of Electrical Engineering (Slovakia), with an engineering degree in III-nitride semiconductors.

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Strong partnerships start with the right people. Our teams combine industry expertise with a deep understanding of your applications. Let's introduce the team!

Meet the CMO Team

- → **Ralph Zoberbier,** *CMO*
- → **Admir Asanoski,** *Head of Business Field Semiconductor & Advanced Packaging*
- → **Jakob Bollhalder,** *Head of Business Field* Compound & Photonics

Our Product Marketing Teams for...

Business Field Semiconductor & Advanced Packaging

Markus Frei	Wafer Level Packaging
Kai Wenz	Frontend
Stanley Low	Panel Level Packaging
Fabian Kramer	Power Devices

Business Field Compound & Photonics

Oguz Yildirim	Wireless
Eduardo Haas	MEMS
Felix Hasler	Discrete LED / Laser & Functional Coatings
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